

Safety-Security Convergence of Industrial Control Systems

« Attacks against SCADA made slightly boring with formal methods »

Maxime PUYS Dec. 13th, 2024



Today's question: How to assess the real impact of cyber-attacks against ICS?



Two Types of IOT

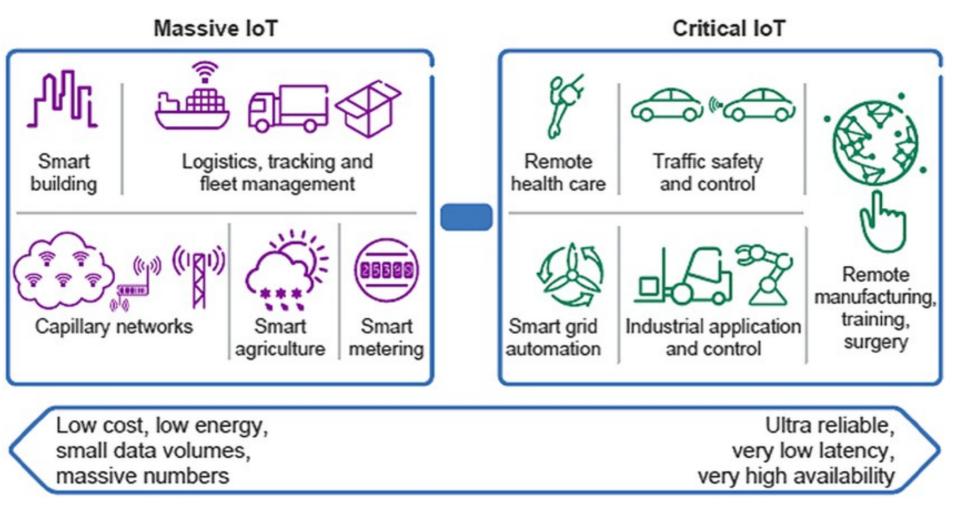




Figure: [Alq19]

Two Types of IOT

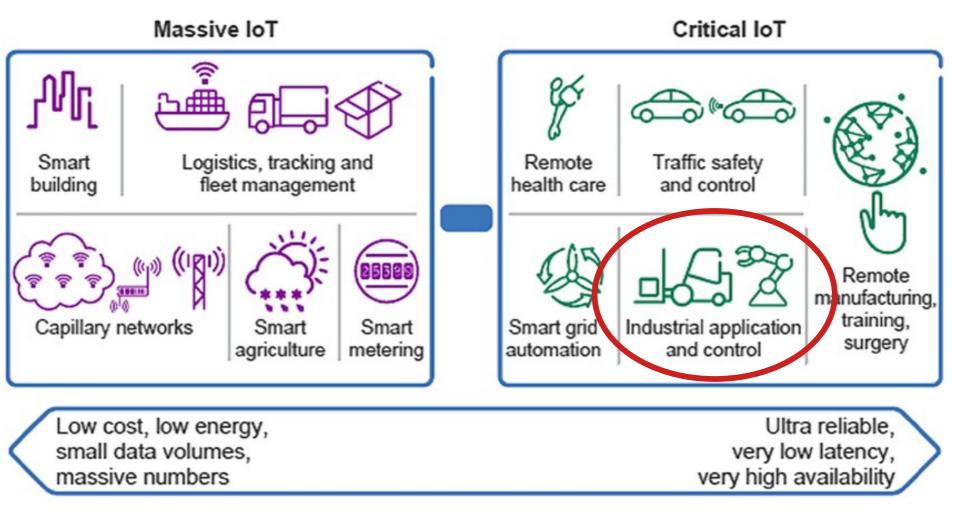
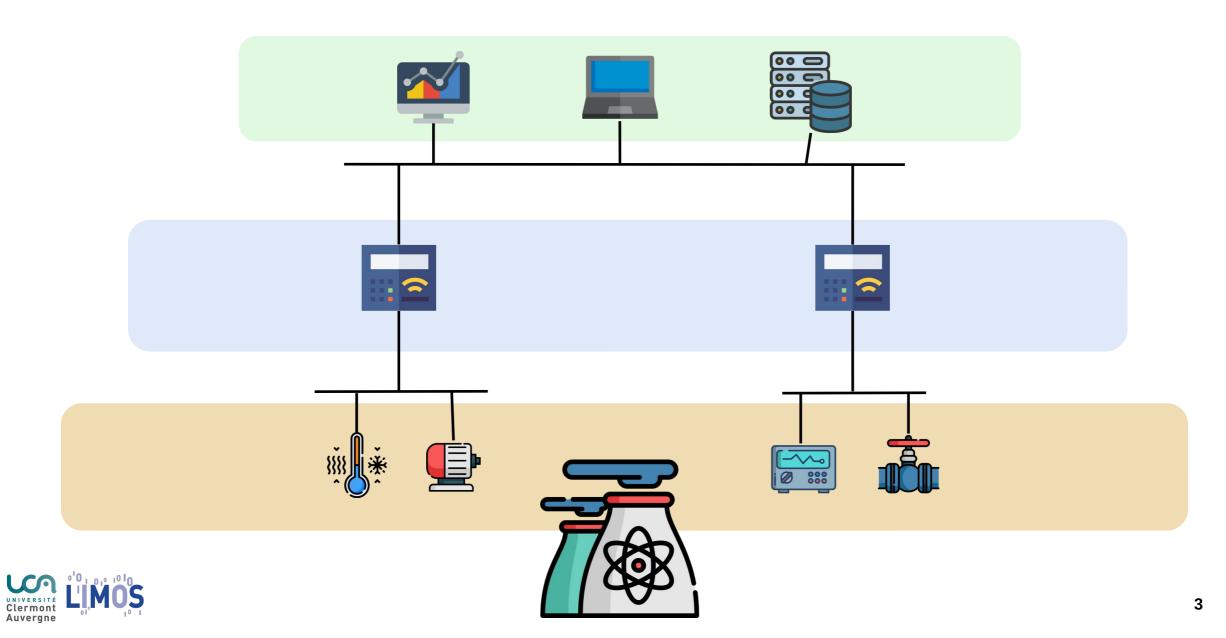


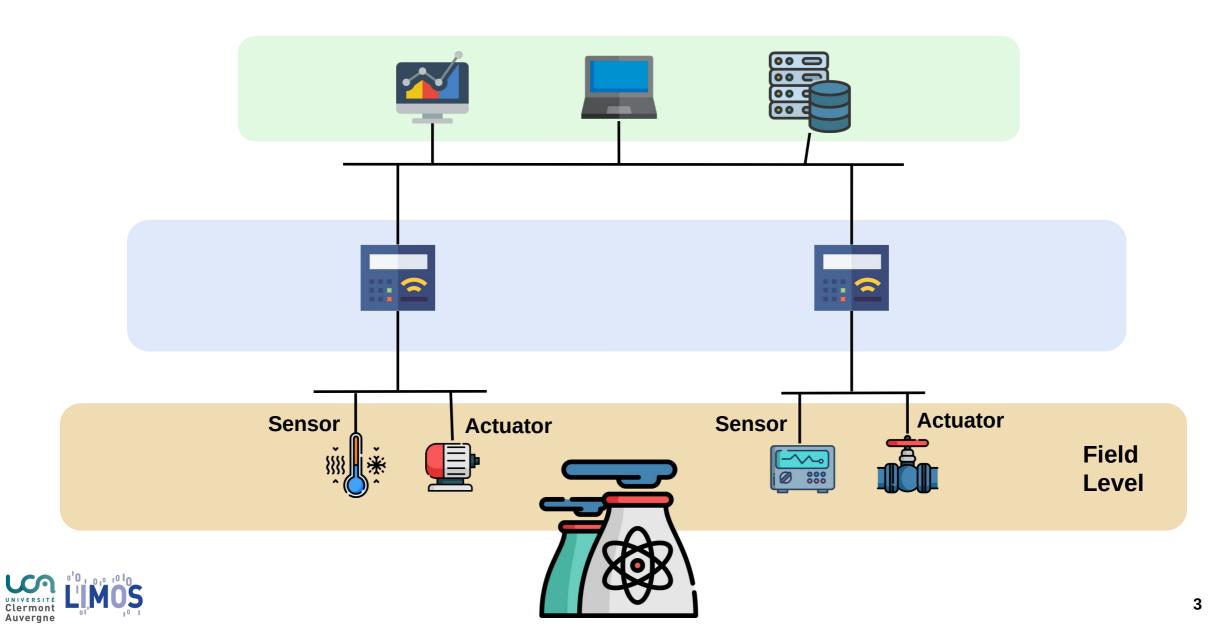


Figure: [Alq19]

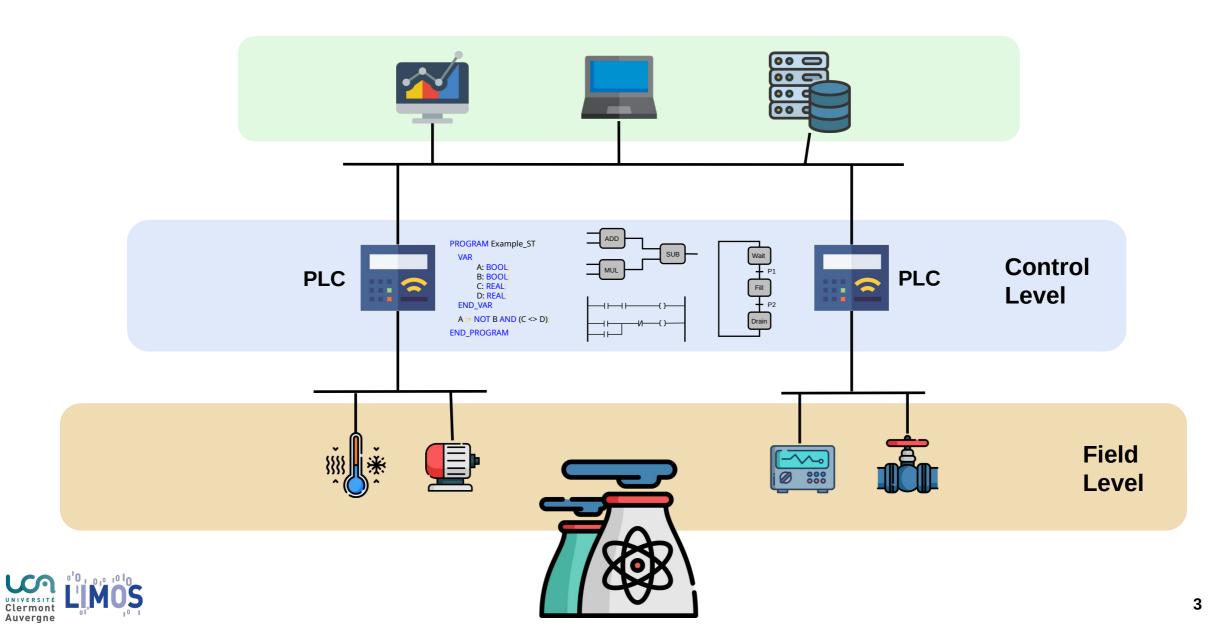


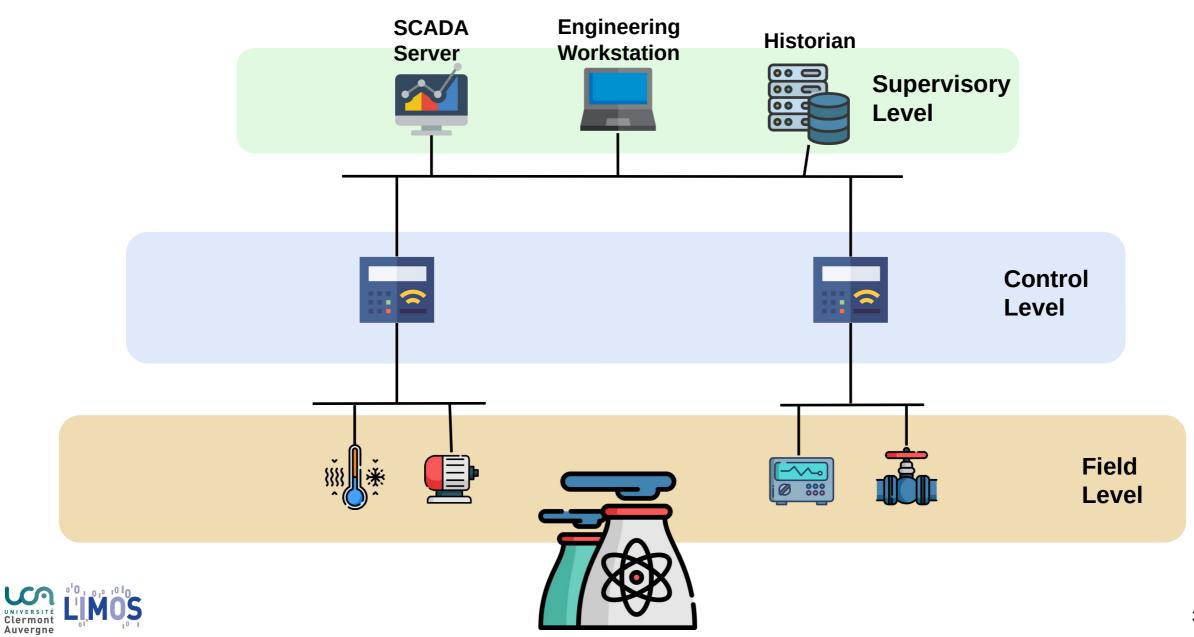






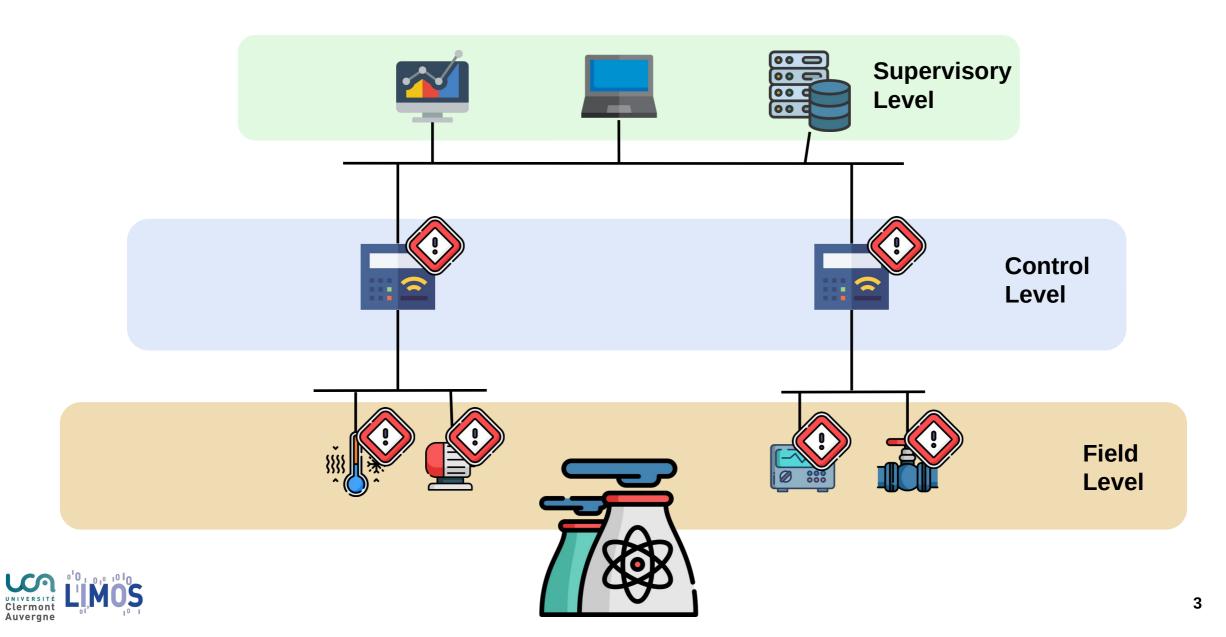




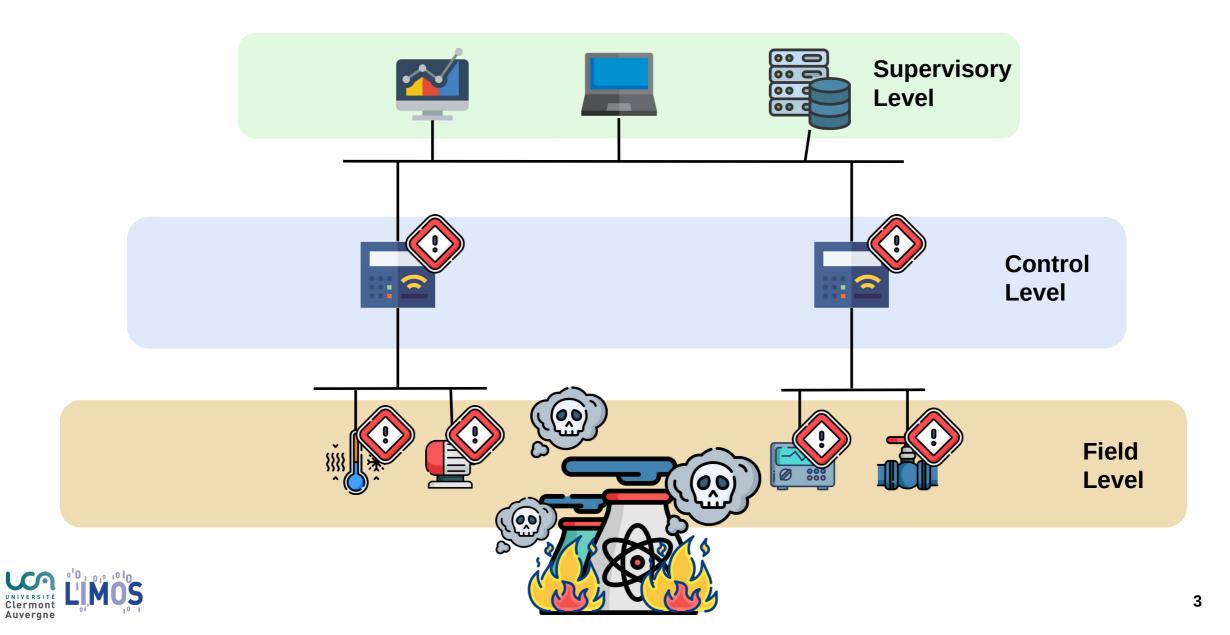


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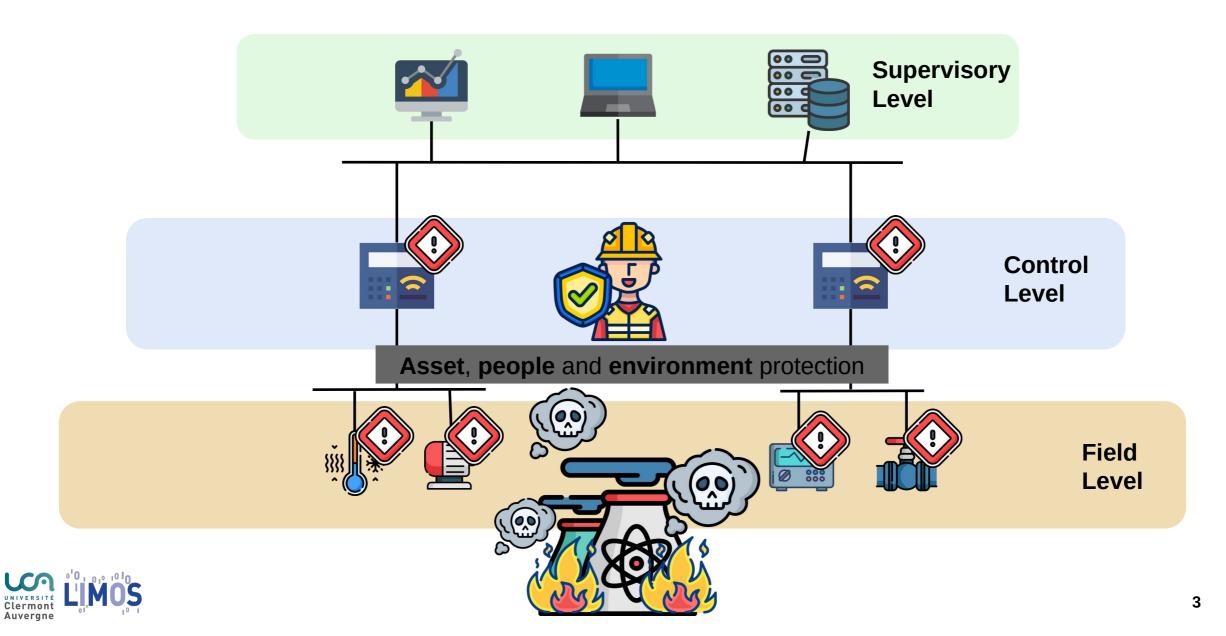




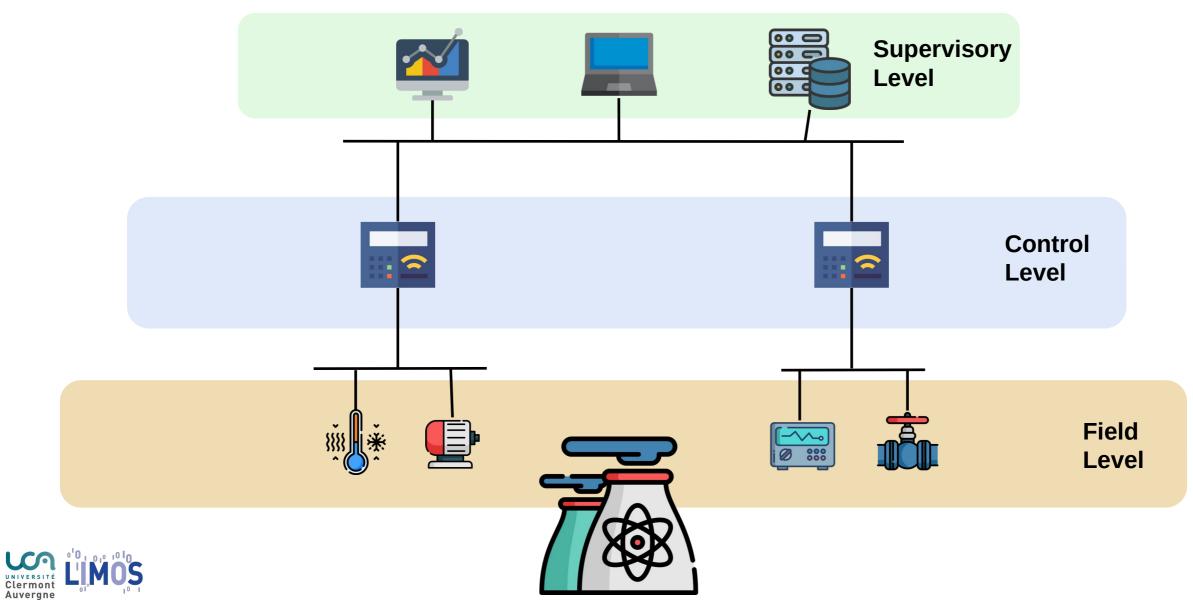




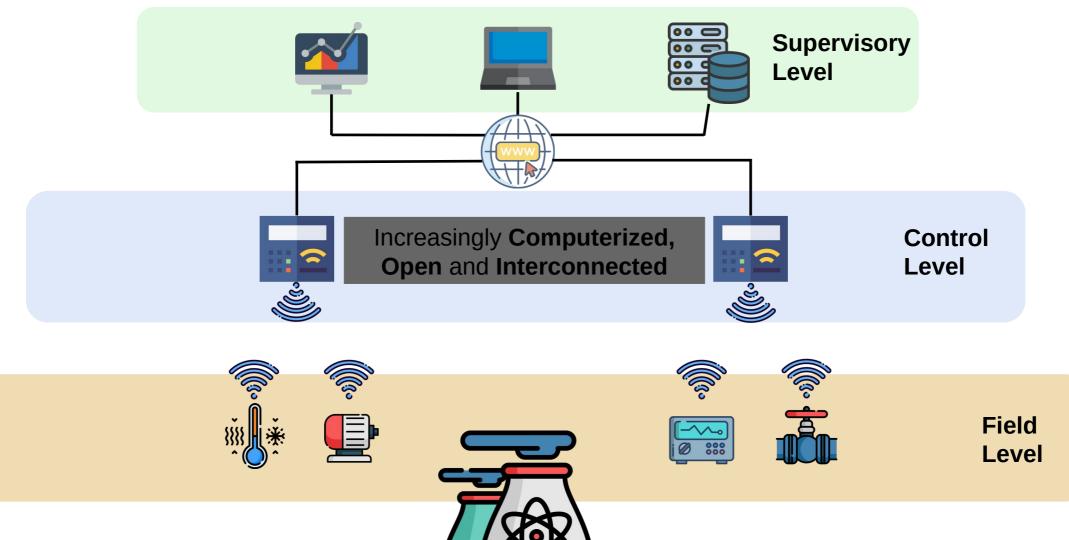






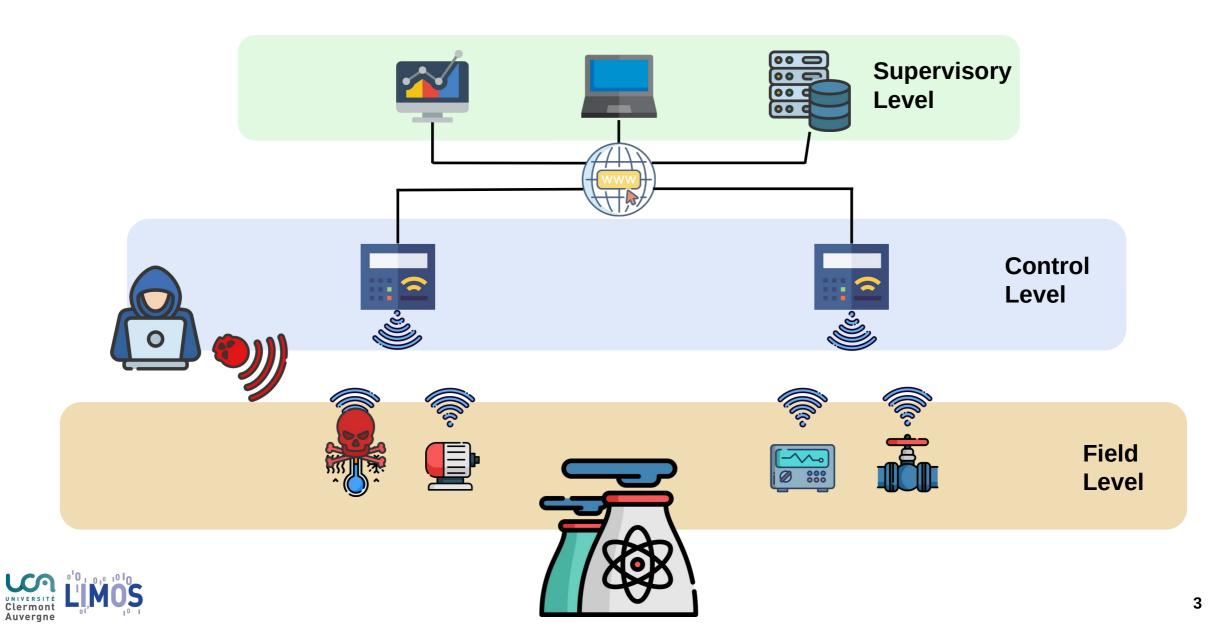




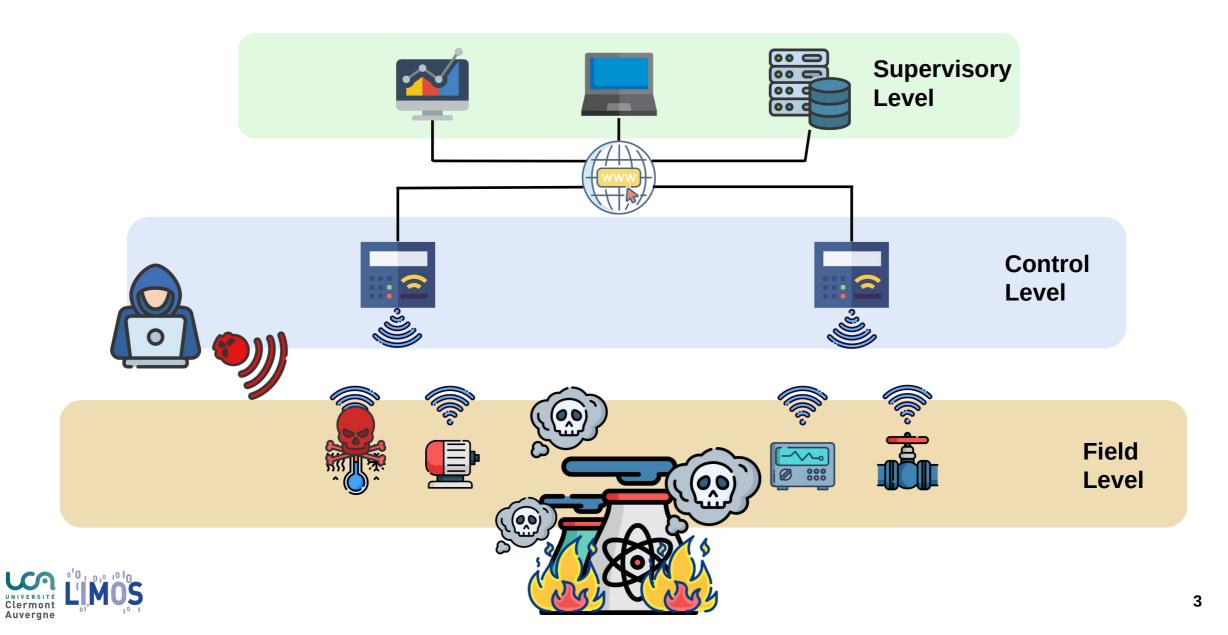








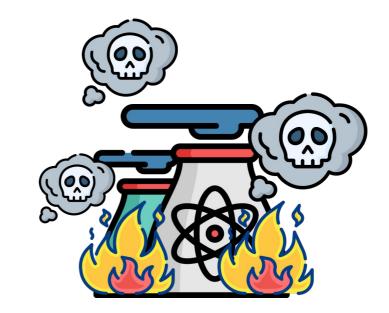




Goal

How to Identify Cyberattacks that Compromise System Safety

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Goal



How to Identify Cyberattacks that Compromise System Safety





Protection against (cyber)**interference** with the proper and intended system **operation**¹ Asset, people and environment protection against process hazards



Contents



Cybersecurity Risk Assessment for System Safety



What an attacker can do



What an attacker might do



Is it serious ?



Literature Review & Classification



Identifying Cybersecurity Risk for System Safety

PLC-Logic Based Cybersecurity Risk Identification . ~



Conclusion and perspectives





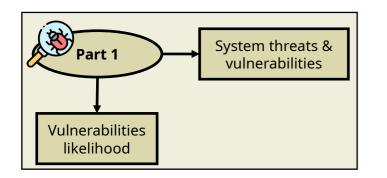


Cybersecurity risk assessment for system safety

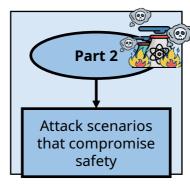
What an attacker <u>can do</u>

What an attacker <u>might do</u>

Is it serious?



Threat modeling tool





Attack scenarios

Risk matrix



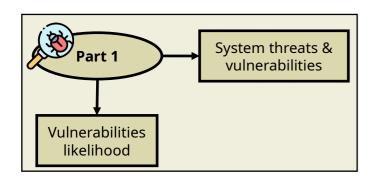


Cybersecurity risk assessment for system safety

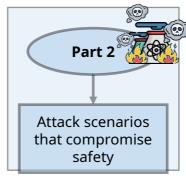
What an attacker <u>can do</u>

What an attacker <u>must do</u>

Is it serious?



Threat modeling tool

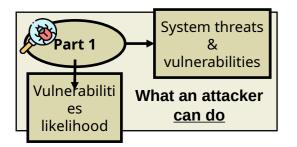




Attack scenarios

Risk matrix





An attacker

Threat modeling

Vulnerabilities



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Threats

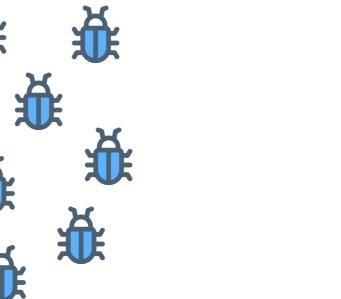
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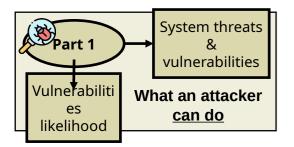
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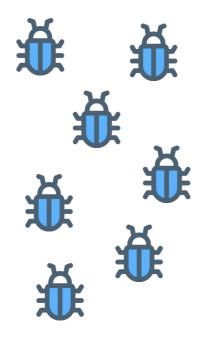




An attacker



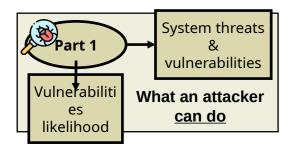
Vulnerabilities



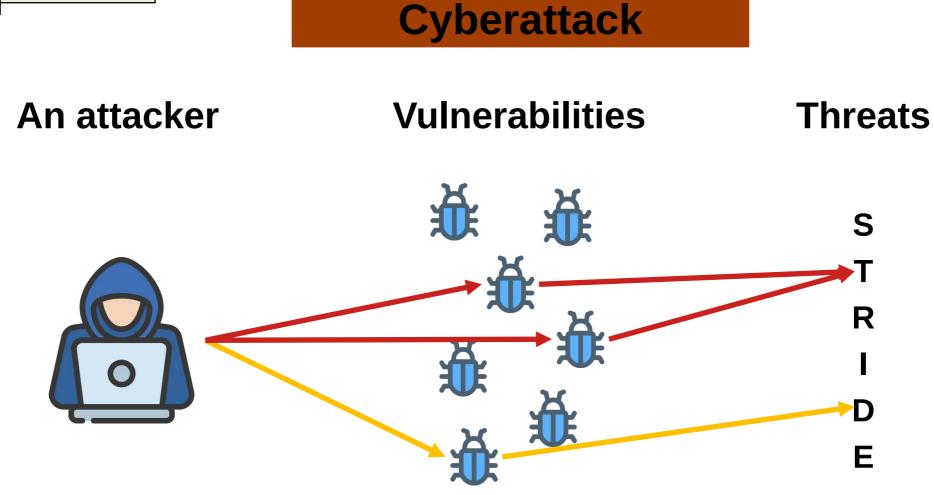
Threats

Spoofing Tampering Repudiation Information disclosure Denial of service Elevation of privilege

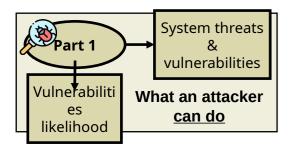








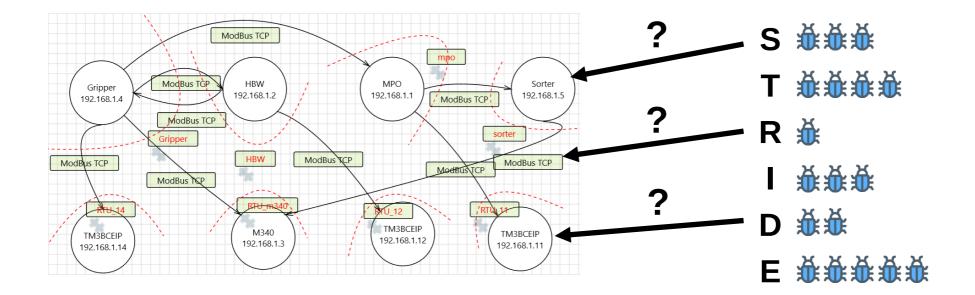




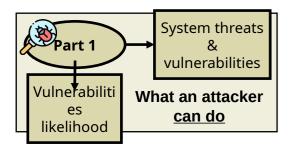


System model





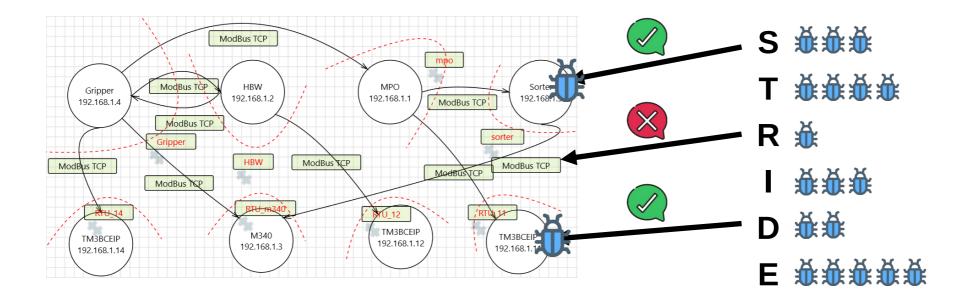






System model

Threats





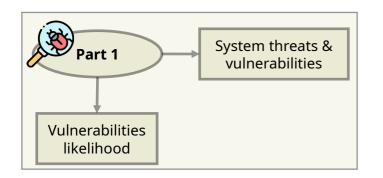


Cybersecurity risk assessment for system safety

What an attacker can do

What an attacker <u>might do</u>

Is it serious?



Threat modeling tool

Part 2 Attack scenarios

that compromise

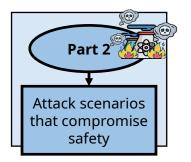
safety



Attack scenarios

Risk matrix

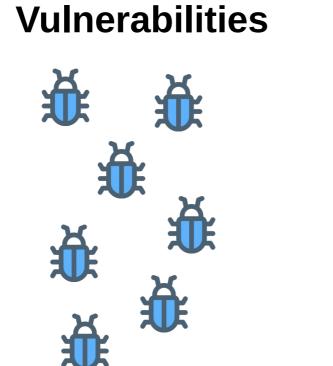




Attack scenarios



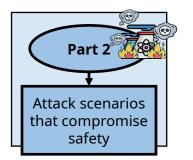
An attacker





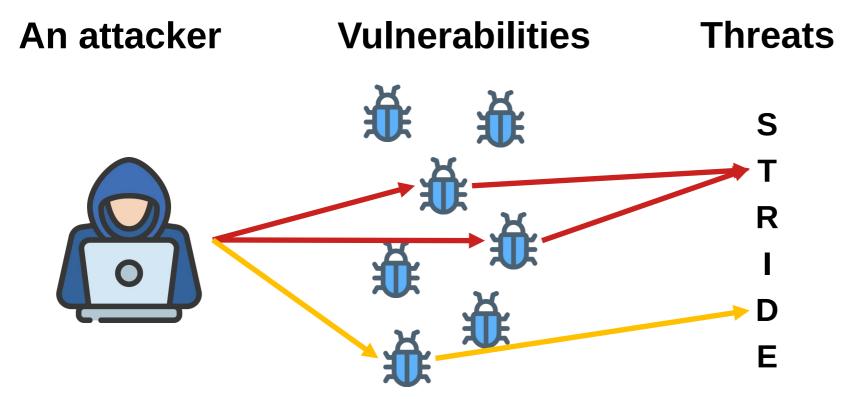
Threats



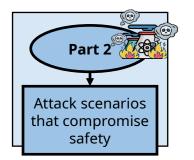


Attack scenarios



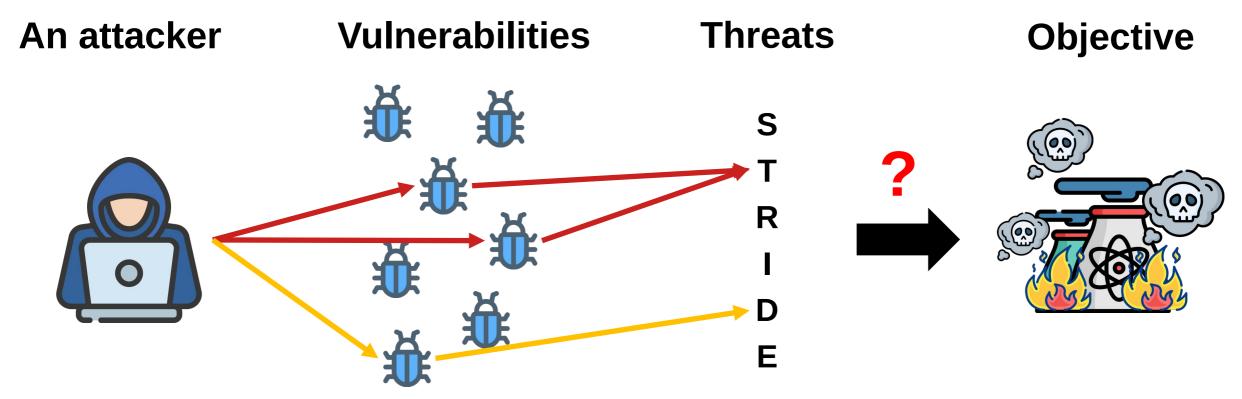




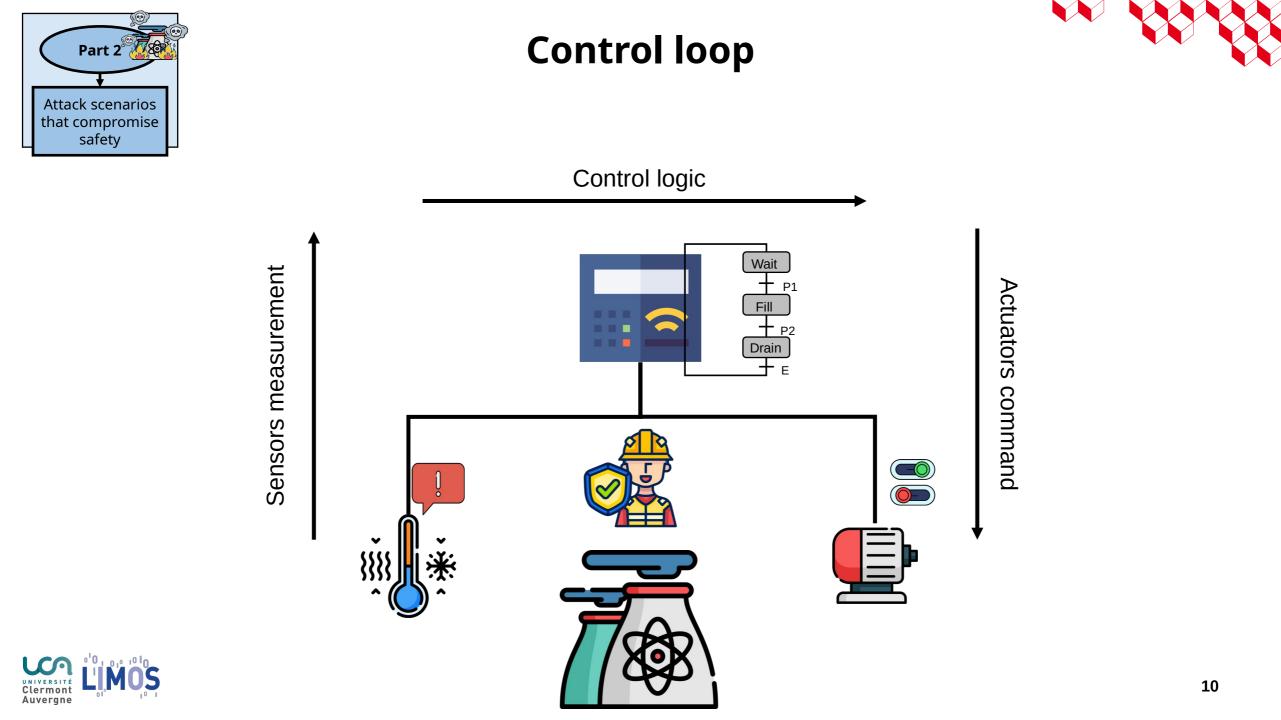


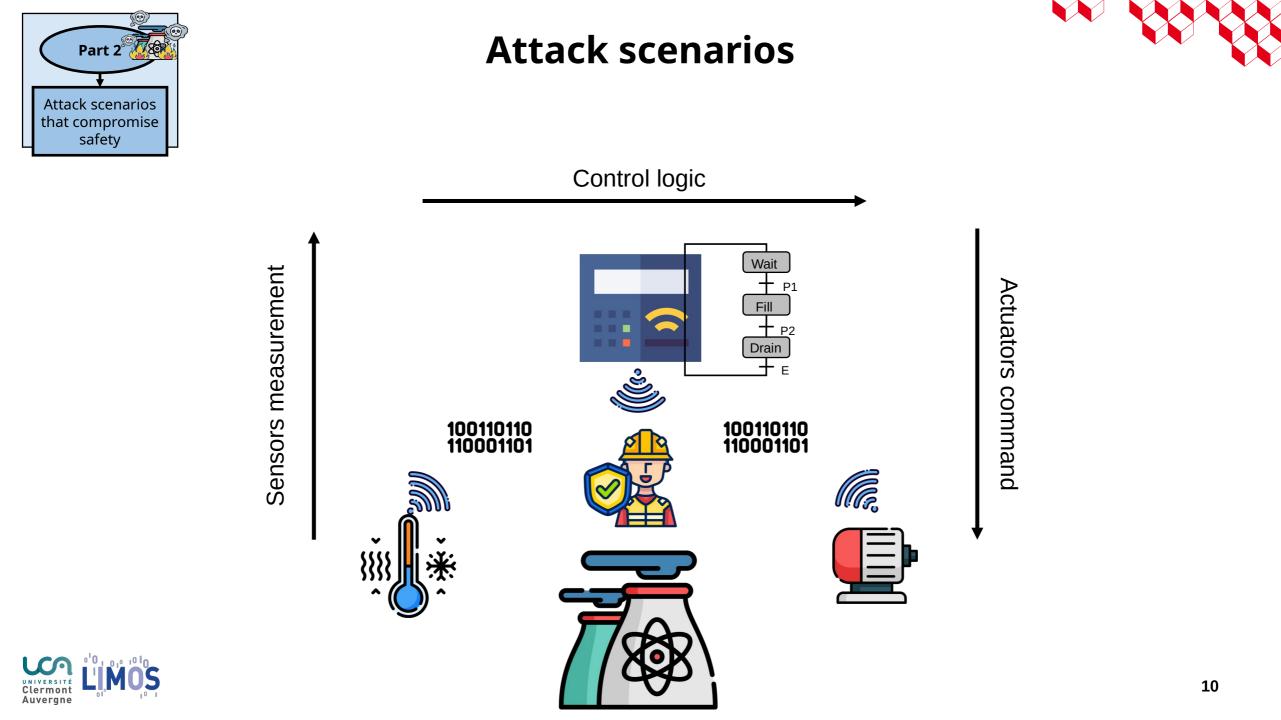
Attack scenarios

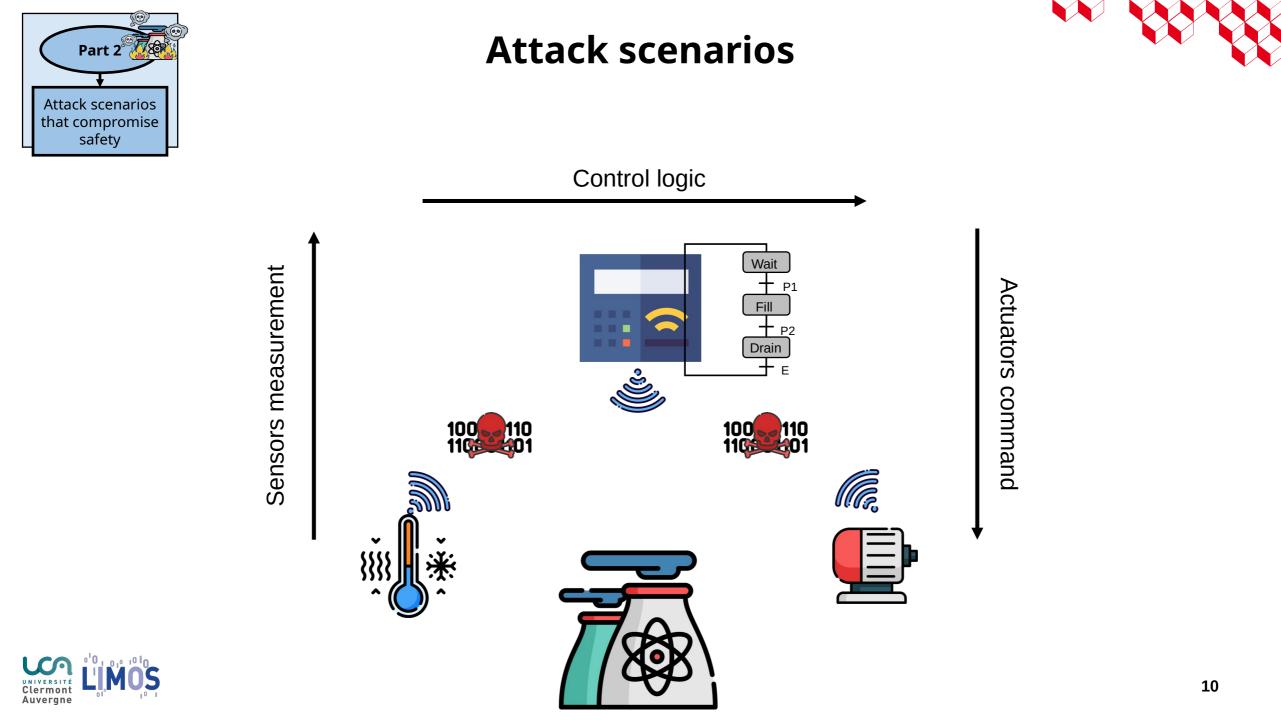


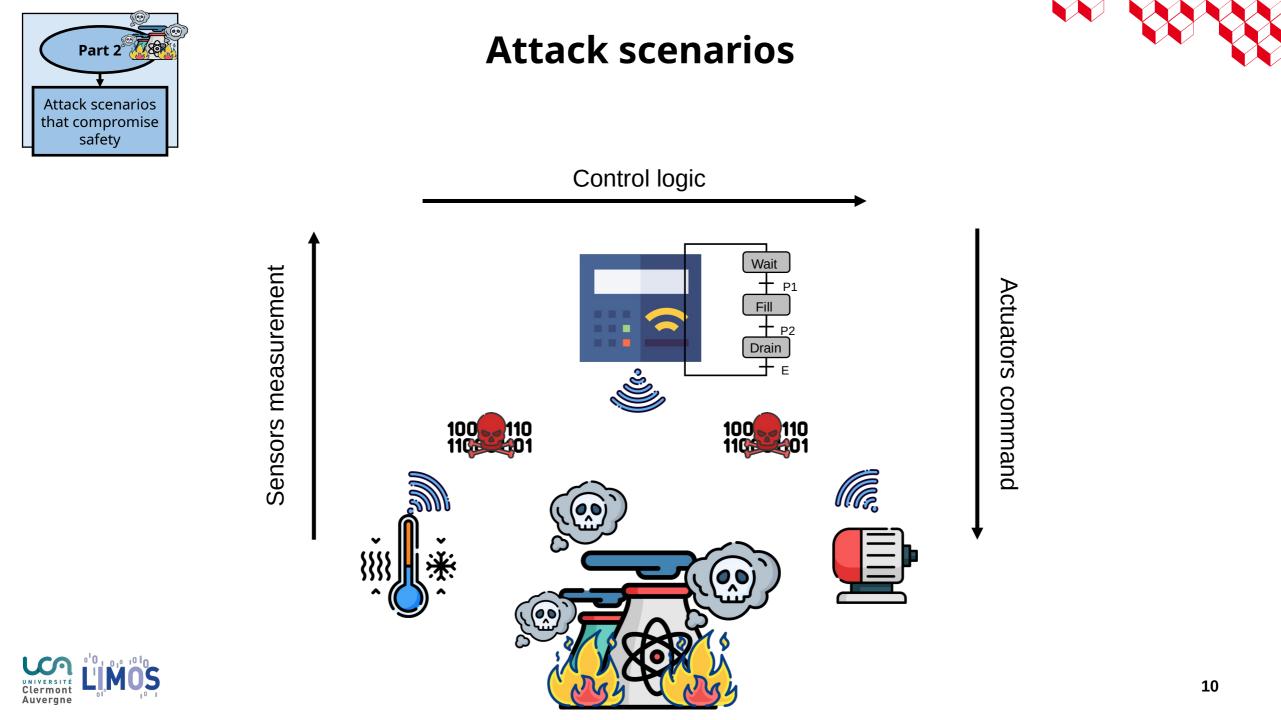












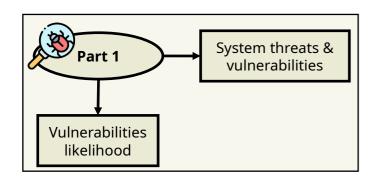


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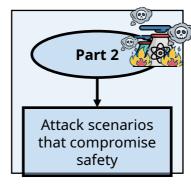
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What an attacker might do

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Threat modeling tool





Attack scenarios

Risk matrix

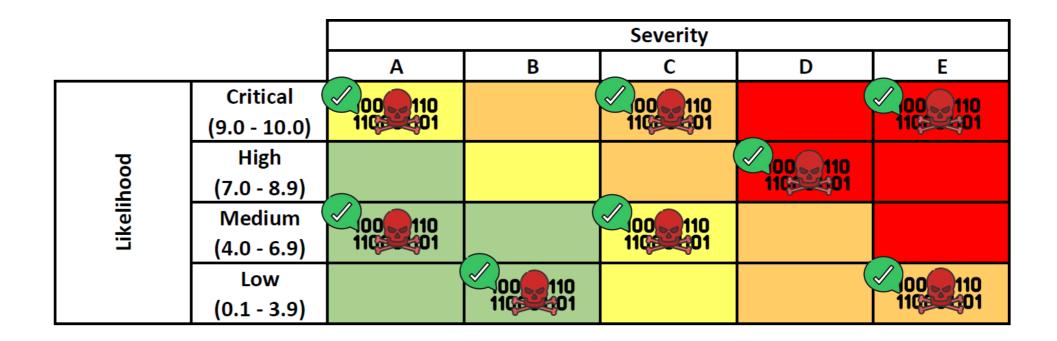




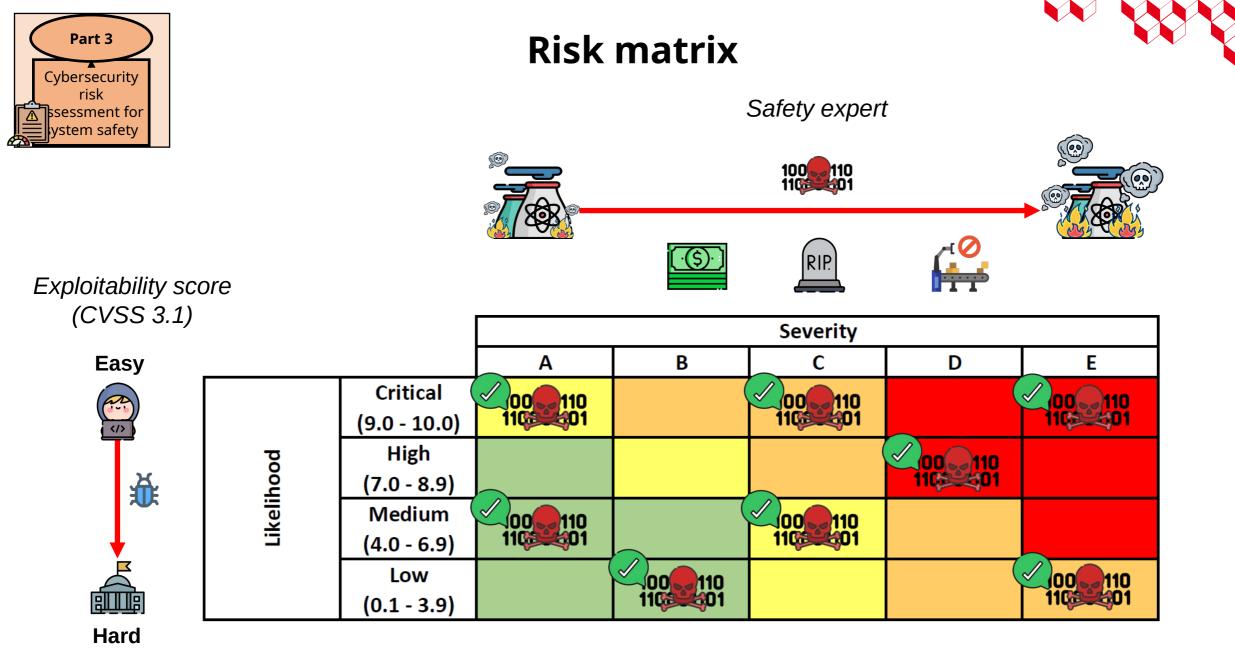
Risk matrix



Standard IEC 62443-3-2/ISO 31010 risk matrix







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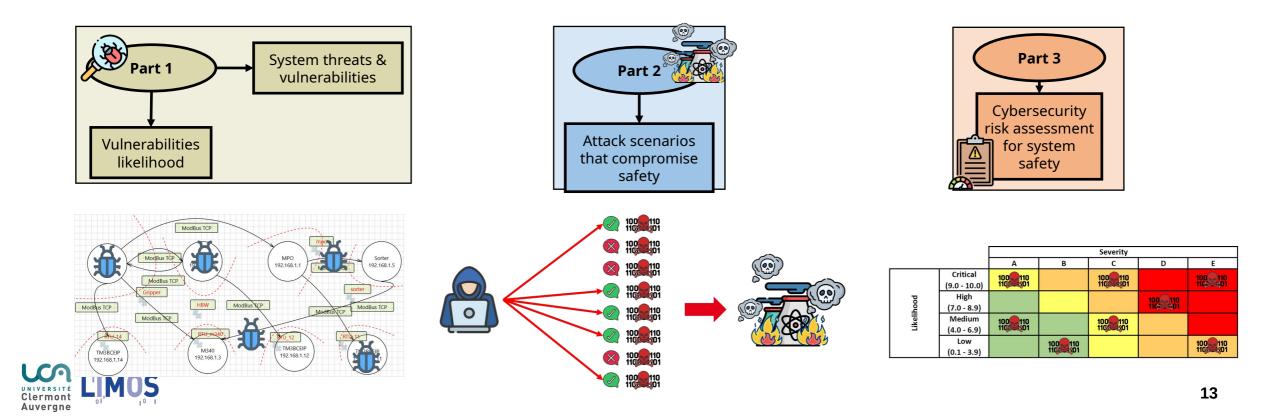


Cybersecurity risk assessment for system safety

What an attacker <u>can do</u>

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Cybersecurity Risk Assessment for System Safety



What an attacker can do



What an attacker might do



Is it serious ?



Example 2 Literature Review & Classification



Identifying Cybersecurity Risk for System Safety

PLC-Logic Based Cybersecurity Risk Identification . ~



Conclusion and perspectives













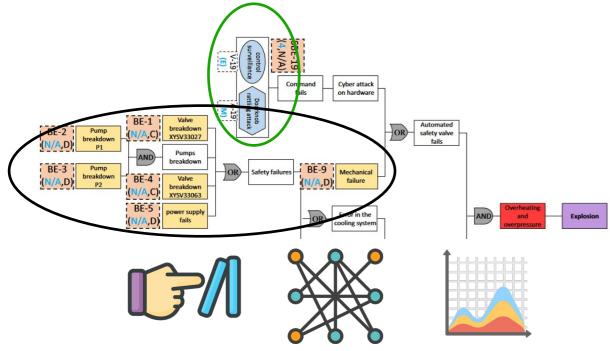








→ Single method

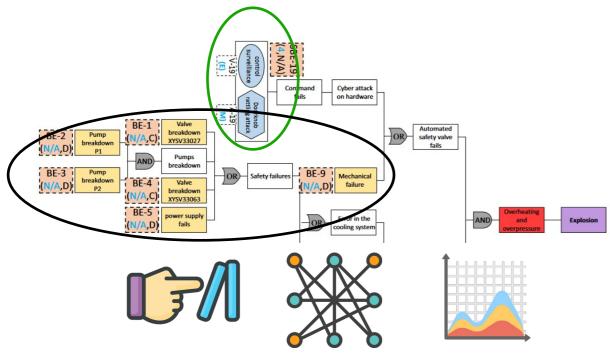








→ Single method





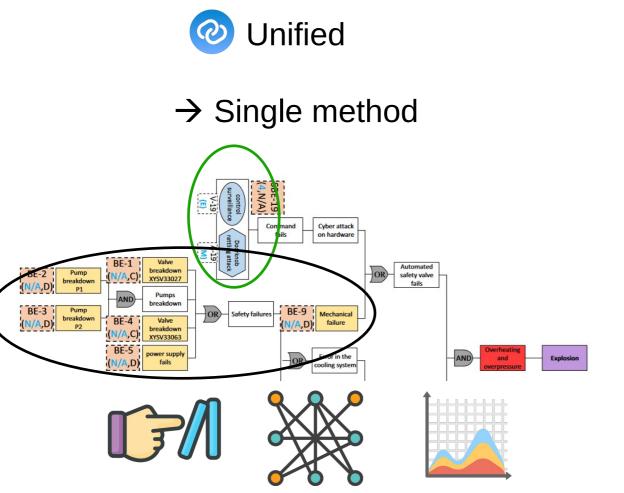
 \rightarrow Separate method







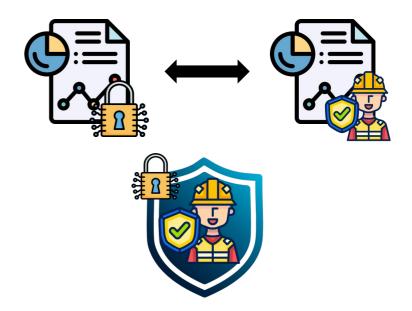








→ Separate method

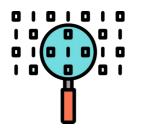


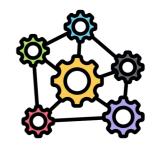




Fine granularity







+20 sensors & actuators

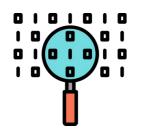


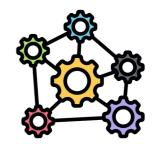




Fine granularity







+20 sensors & actuators





Methods	Integrated	System Size	Methods	Integrated	System Size
Winther et al. (2001)	✓	Small	Subramanian et Zalewski (2018)	×	Small
Cárdenas et al. (2011)	\checkmark	Small	Puys et al. (2018)	\checkmark	Small
Song et al. (2012)	\checkmark	Small	Zhu et al. (2018)	\checkmark	Small
Young et Leveson (2013)	\checkmark	Small	Papakonstantinou et al. (2019)	×	Small
Kriaa (2015)	×	Small	Khaled et al. (2020)	\checkmark	Small
Sabaliauskaite et al. (2015)	×	Small	Kumar et al. (2020)	×	Small
Mesli-kesraoui et al. (2016)	✓	Small	Hosseini et al. (2021)	×	Small
Subramanian et Zalewski (2016)	×	Small	Oueidat et al. (2021)	×	Small
Rocchetto et Tippenhauer (2017)	✓	Large	Bhosale et al. (2023)	\checkmark	Small
Friedberg et al (2017)	×	Small	Eckhart et al. (2022)	\checkmark	Small
Abdo et al. (2018)	×	Small	Földvári et al. (2023)	×	Small
Cheh et al. (2018)	√	Small	Son et al. (2023)	\checkmark	Small
			This work	\checkmark	Large



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Literature Review & Classification



Identifying Cybersecurity Risk for System Safety

PLC-Logic Based Cybersecurity Risk Identification . ~



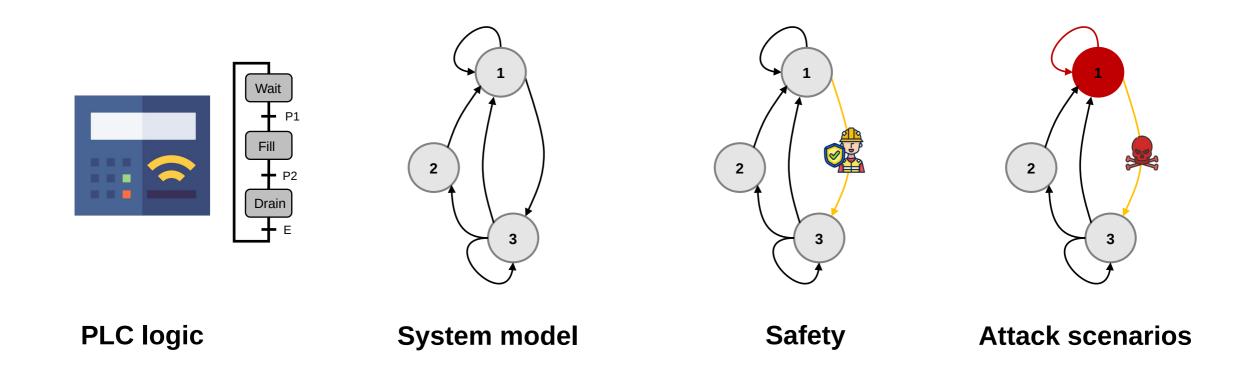
Conclusion and perspectives







PLC-Logic Based Cybersecurity Risk Identification

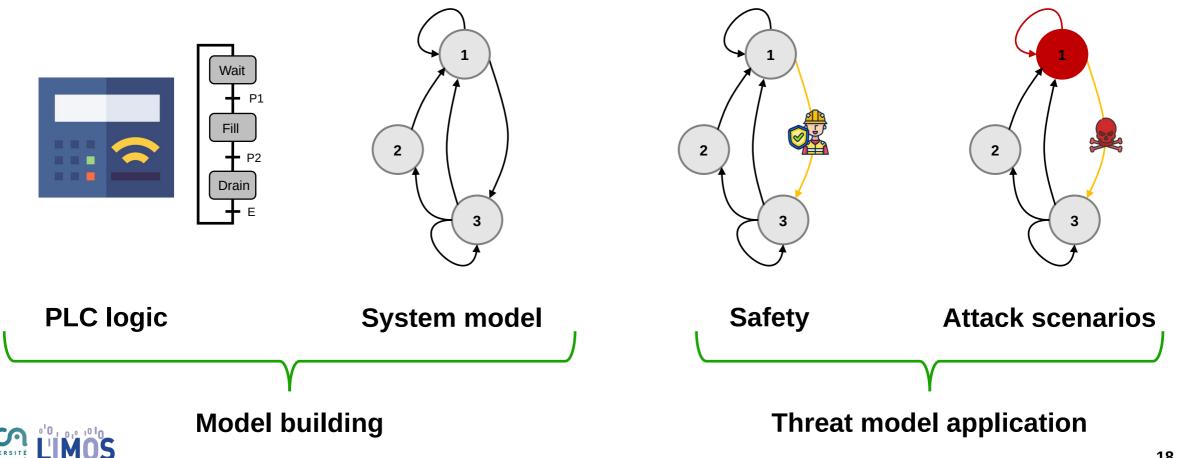






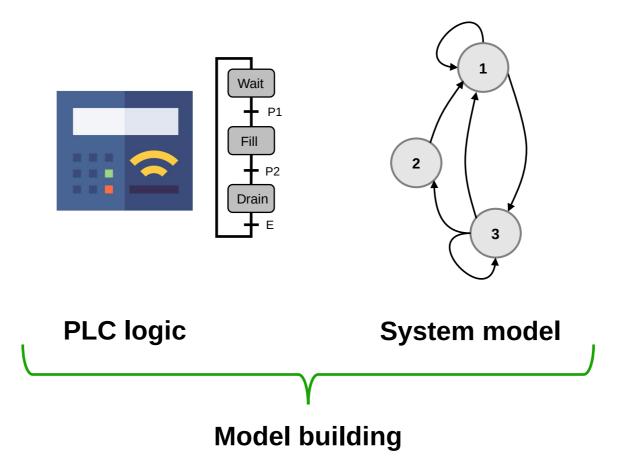
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PLC-Logic Based Cybersecurity Risk Identification





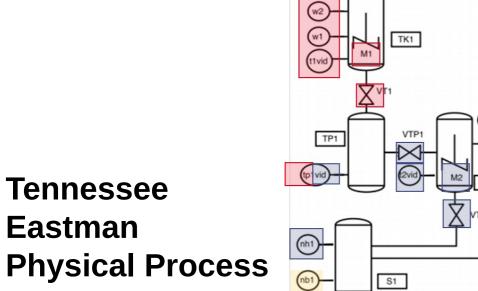


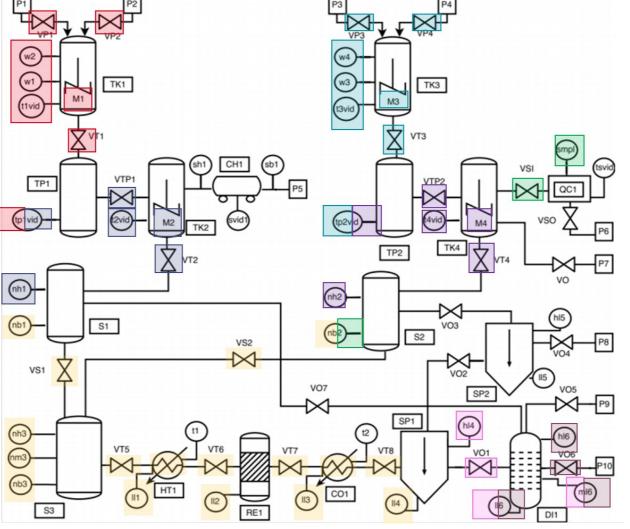




Objective







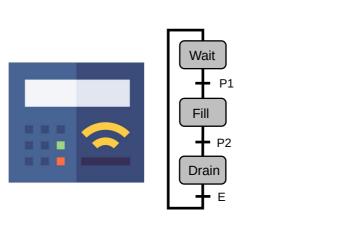
26 sensors24 actuators

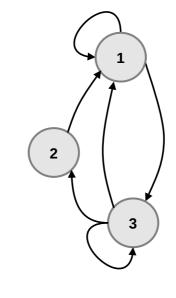


McAvoy, T. J., & Ye, N. (1994). Base control for the Tennessee Eastman problem. Computers & Chemical Engineering, 18(5), 383-413.







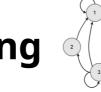


PLC logic

System model



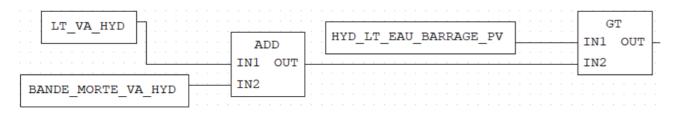


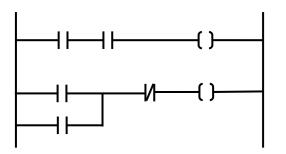


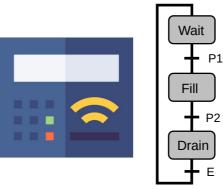


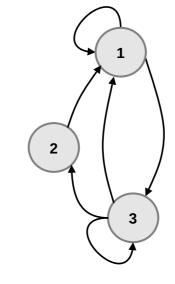
P1

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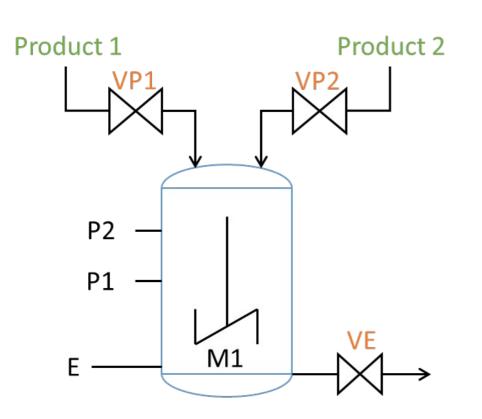
PROGRAM Example_ST VAR A: BOOL; B: BOOL; C: REAL; D: REAL; END_VAR A := NOT B AND (C <> D);END_PROGRAM

Sequential Function Chart (SFC)

System model



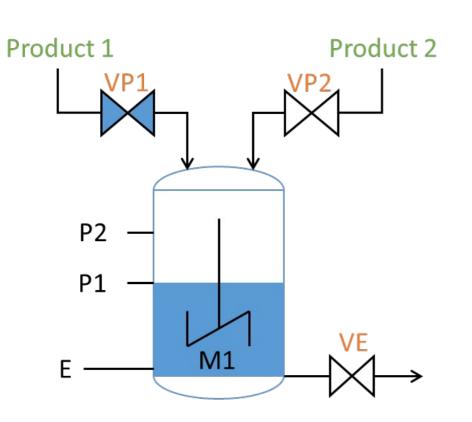


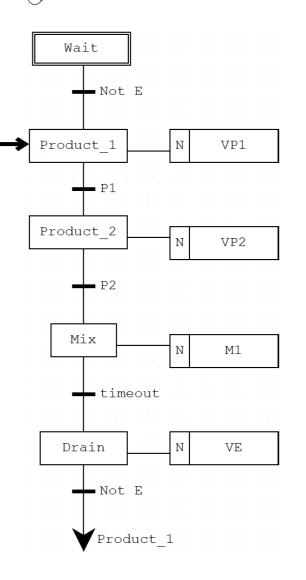


Wait			
Not E			
Product_1	N	VP1	
P1	· · ·	· · · · · · · · · · ·	
Product_2		VP2	
P2	· · · · · · · · · · · · · · · · · · ·		
Mix	N	M1	
- timeout	 	· · · · · · · · · · · · · · · · · · ·	
Drain		VE	
Not E	· ·	· · · · · · · · · · ·	
Product	1		





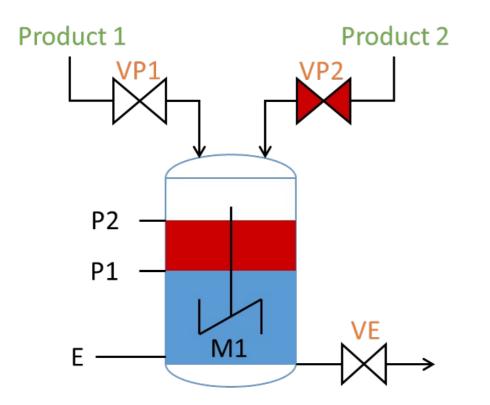


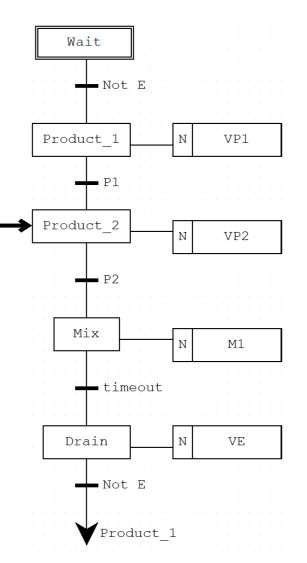






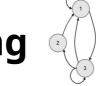


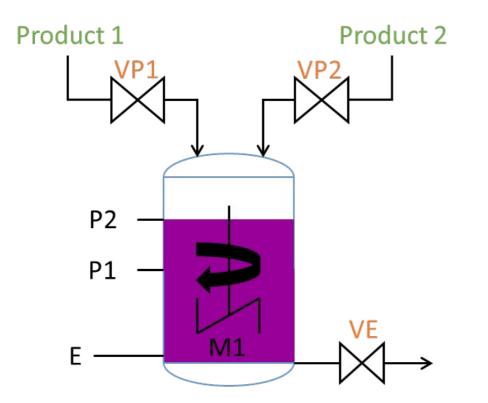


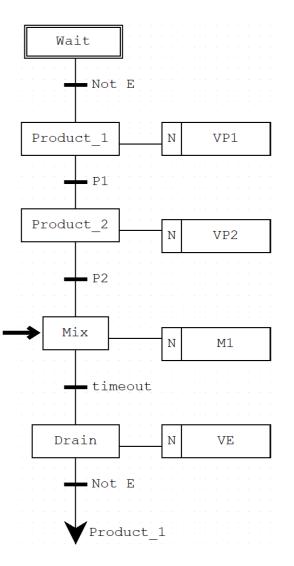








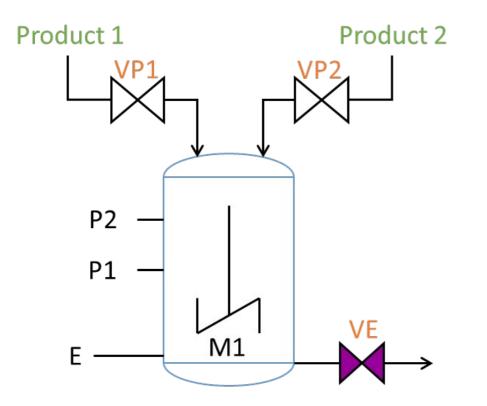


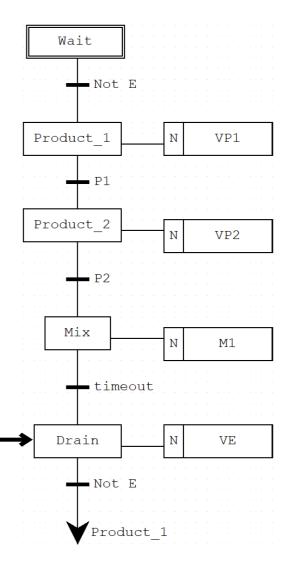






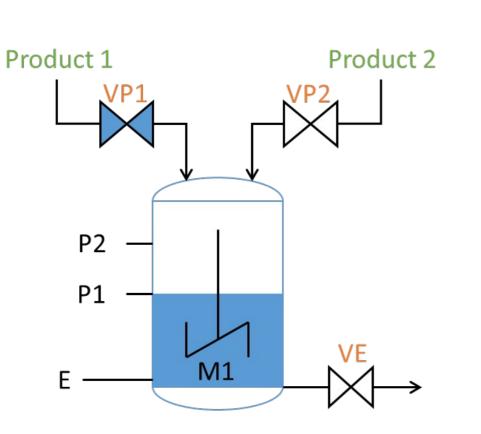


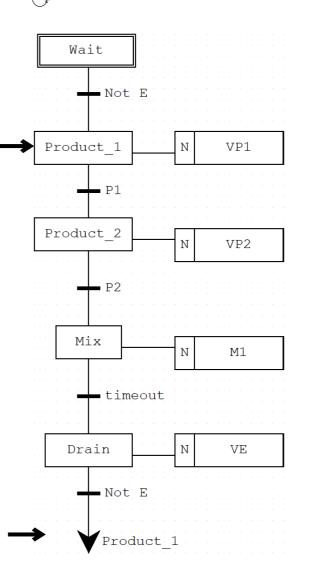




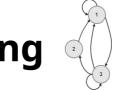




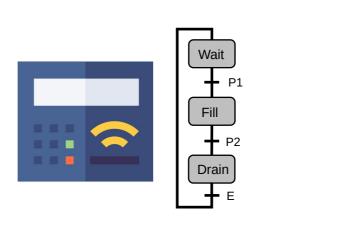


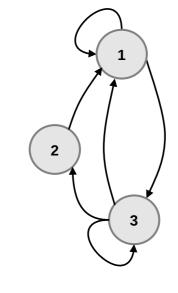












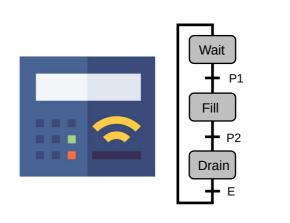
SFC

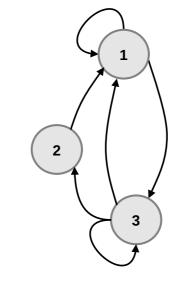
System model









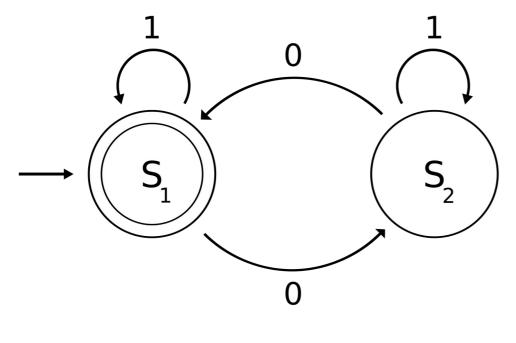


SFC

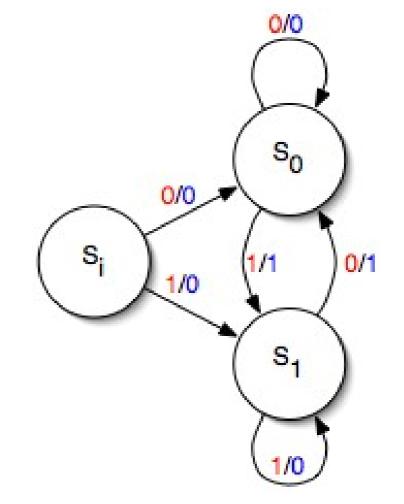
Finite-state transducer







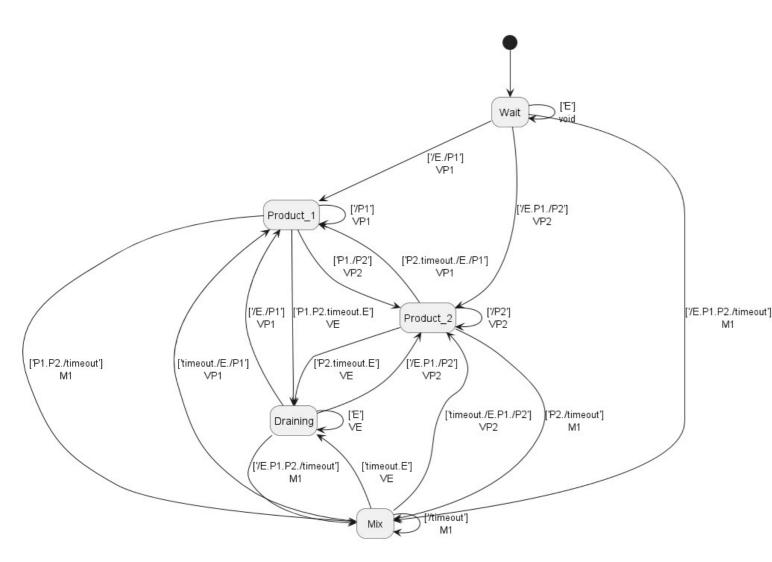
Finite State Machine

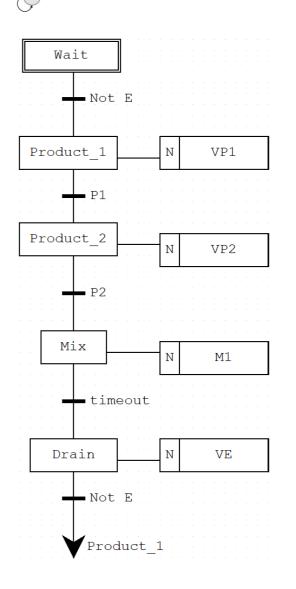


Finite State Transducer Mealy Machine



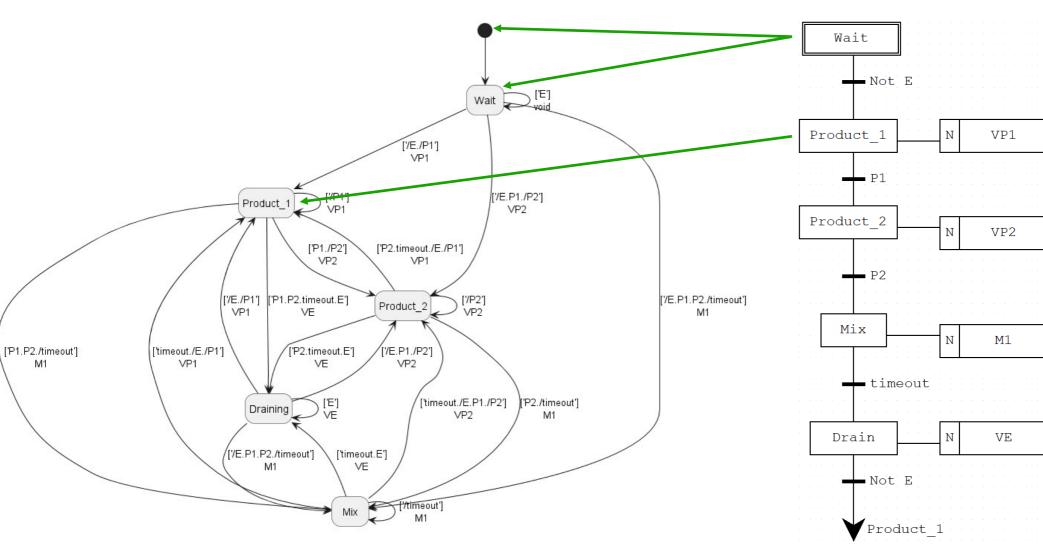






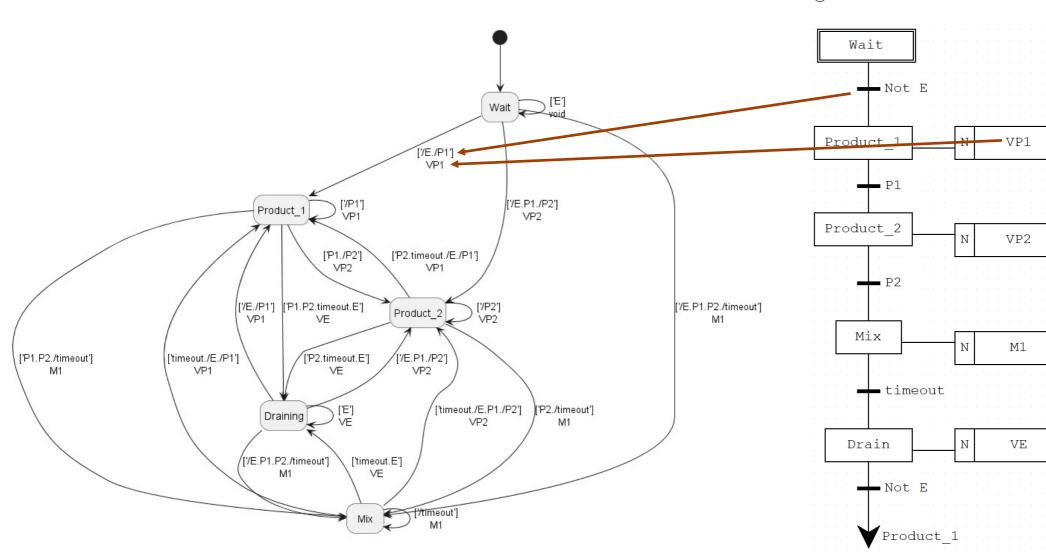






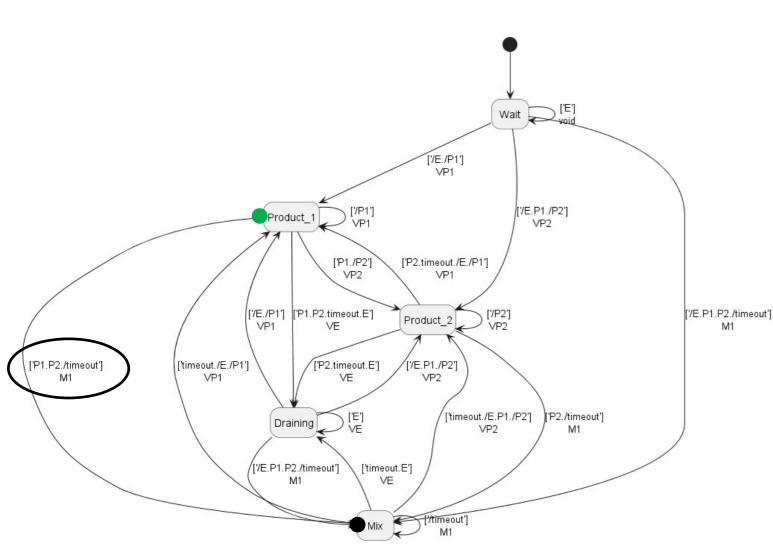


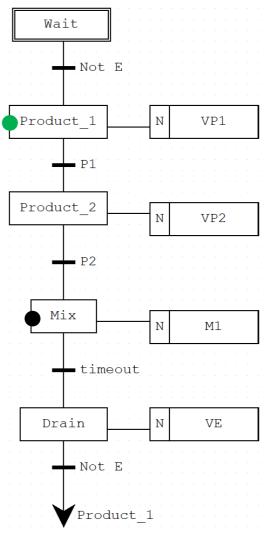












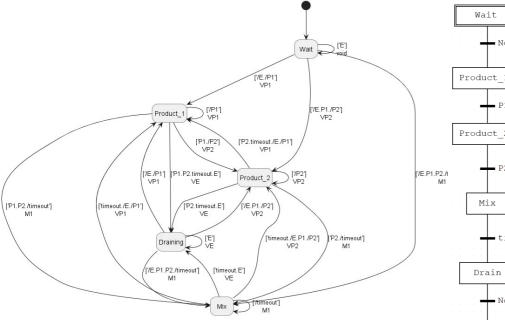


Calculate once upstream

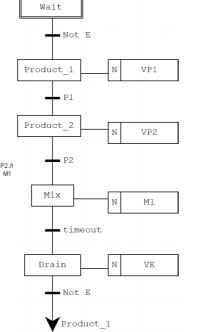
Calculate each time

Objective

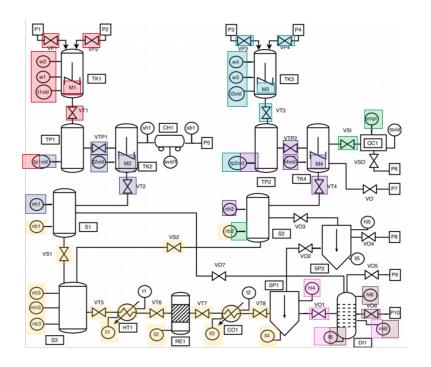




5 states





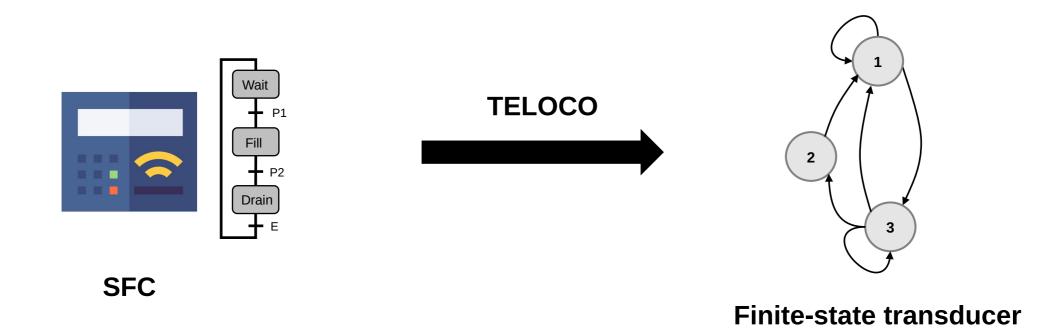


6.7 x 10⁵ states



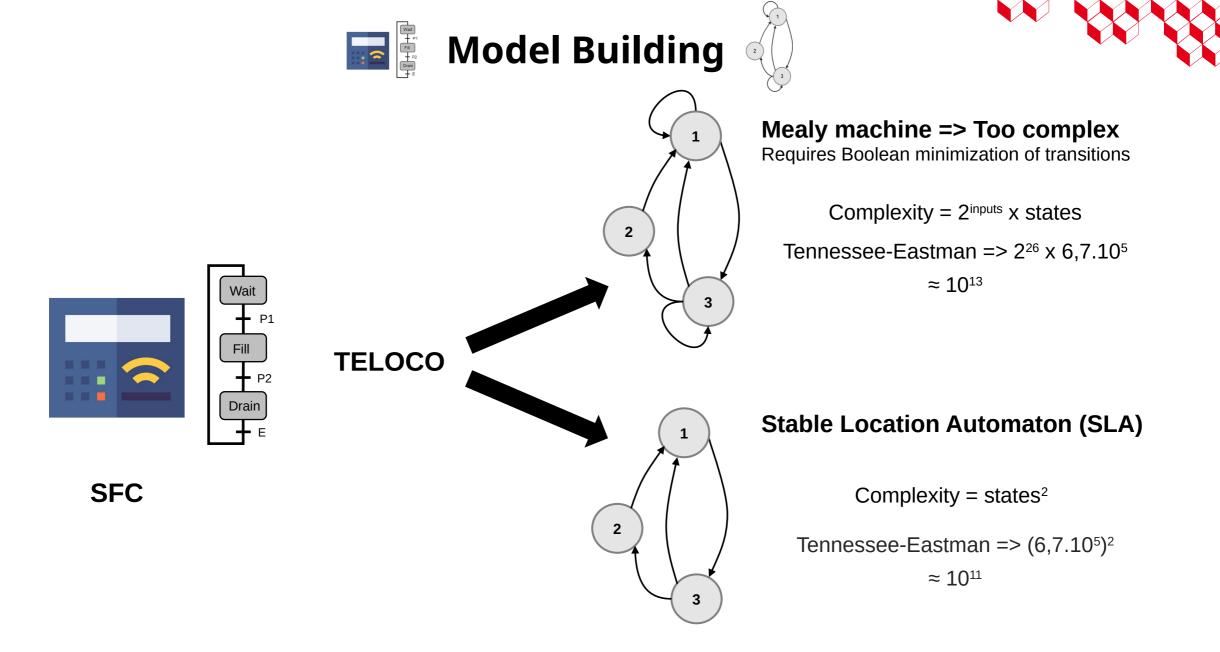








J. Provost, J.-M. Roussel, et J.-M. Faure, « Translating Grafcet specifications into Mealy machines for conformance test purposes », *Control Engineering Practice*, sept. 2011, doi: <u>10.1016/j.conengprac.2010.10.001</u>.









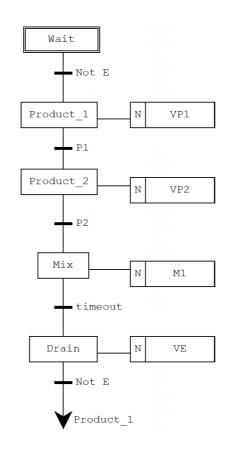
Modeling Time

	SLA	Mealy	Minimization	Inputs
	1 ms	0 ms	372 ms	3
	0 ms	0 ms	376 ms	4
	0 ms	0 ms	382 ms	5
	141 ms	51 ms	505 ms	9
	42 ms	162 ms	17 219 ms	13
	21 973 ms	30 190 ms	65 813 ms	13
	1 320 ms	15 143 ms	1 381 511 ms	16
	2 625 ms	46 875 ms	X	17
	50 036 ms	994 192 ms	X	18
	1 091 838 ms	X	Х	18
Tennessee-Eastman	→ X	X	X	26

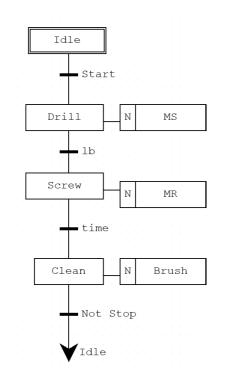


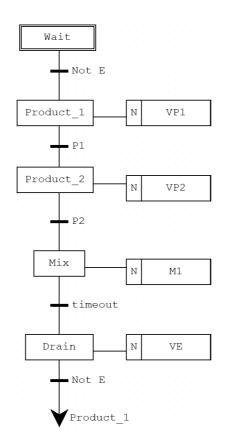
→ Intel(R) Core(TM)i5-8365U @1,60GHz-1,90GHz and 16 Go of RAM.

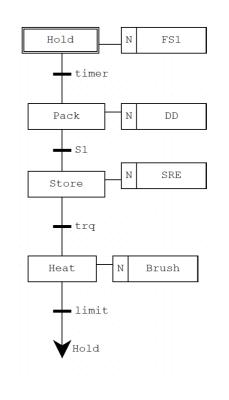






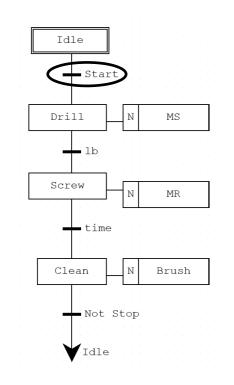


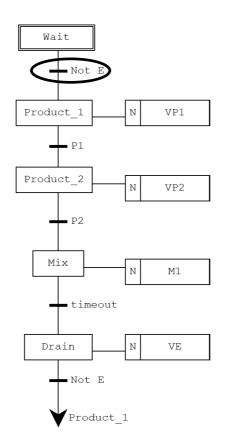


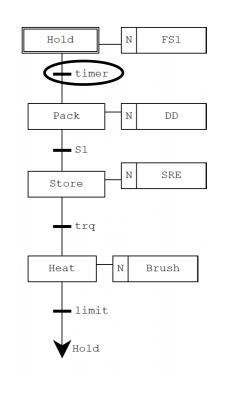


/!\ Not one big SFC but multiple smaller running at the same time



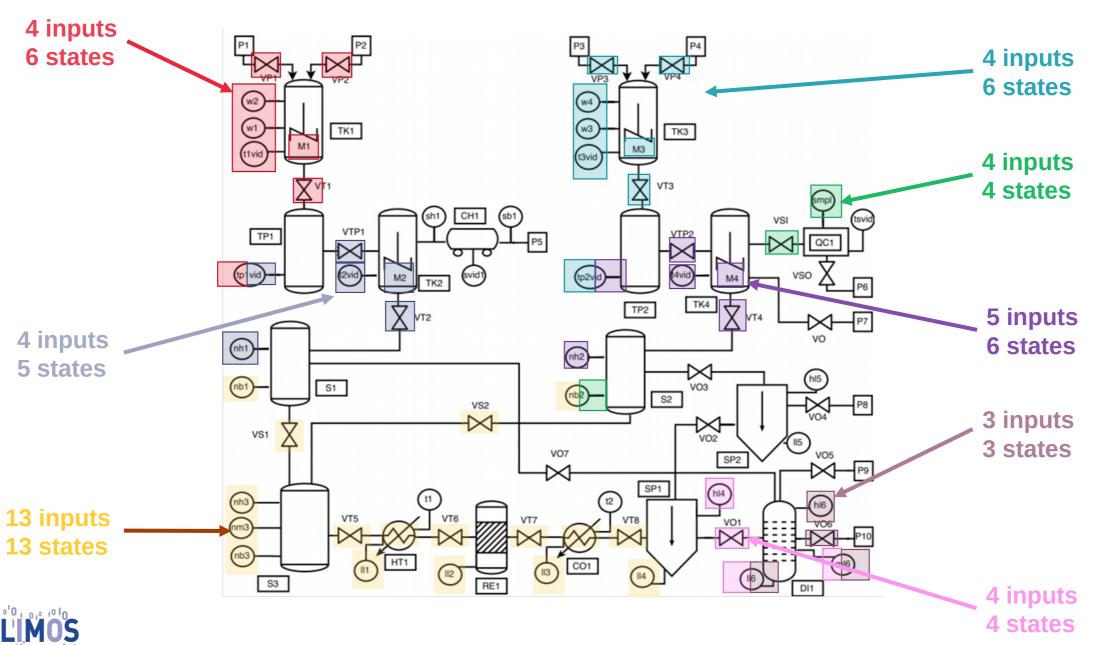






/!\ In the worst case, # states is not the sum of all states but the product

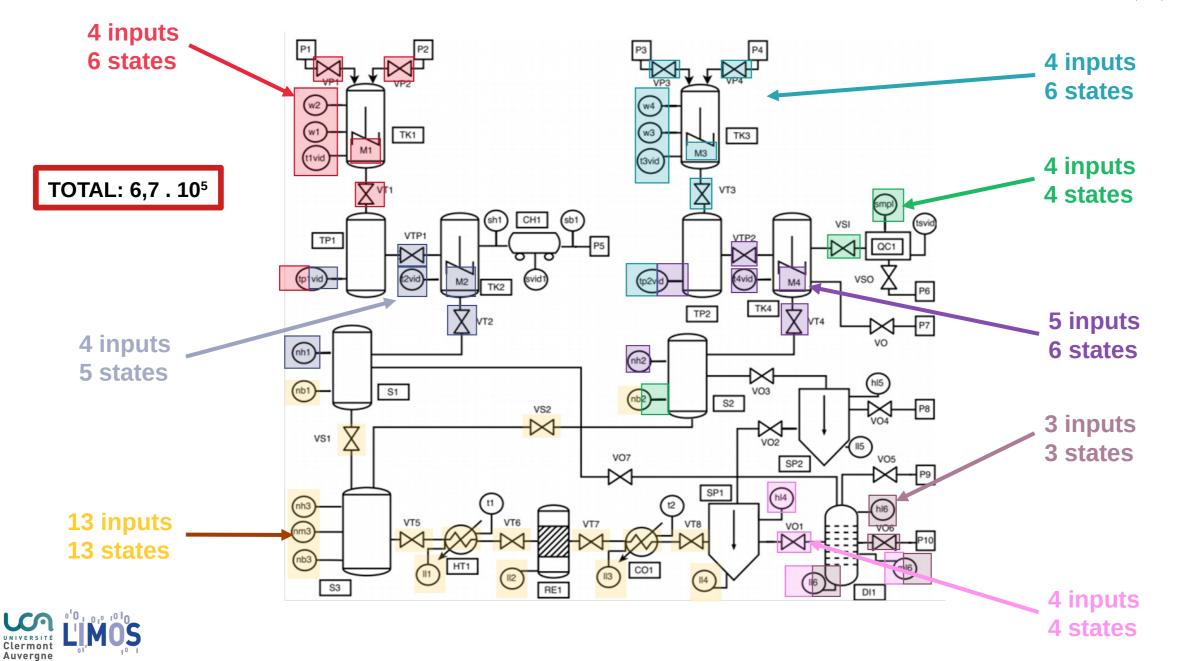




Clermont

Auvergne

28







	SLA	Graphs	Inputs
	1 ms	1	3
	0 ms	1	4
	0 ms	1	5
	42 ms	1	13
	141 ms	2	9
1 320 ms		2	16
2 625 ms		2	17
21 973 ms		3	13
50 036 ms		3	18
1 091 838 ms		4	18
Х		8	26







SLA	Graphs	Inputs
1 ms	1	3
0 ms	1	4
0 ms	1	5
42 ms	1	13
141 ms	2	9
1 320 ms	2	16
2 625 ms	2	17
21 973 ms	3	13
50 036 ms	3	18
1 091 838 ms	4	18
Х	8	26







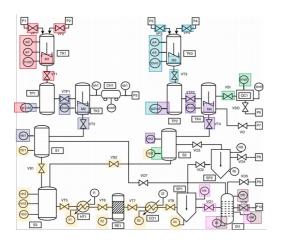
SLA	Graphs	Inputs
1 ms	1	3
0 ms	1	4
0 ms	1	5
42 ms	1	13
141 ms	2	9
1 320 ms	2	16
2 625 ms	2	17
21 973 ms	3	13
50 036 ms	3	18
1 091 838 ms	4	18
Х	8	26





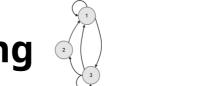


SLA	Graphs	Inputs
1 ms	1	3
0 ms	1	4
0 ms	1	5
42 ms	1	13
141 ms	2	9
1 320 ms	2	16
2 625 ms	2	17
21 973 ms	3	13
50 036 ms	3	18
1 091 838 ms	4	18
Х	8	26

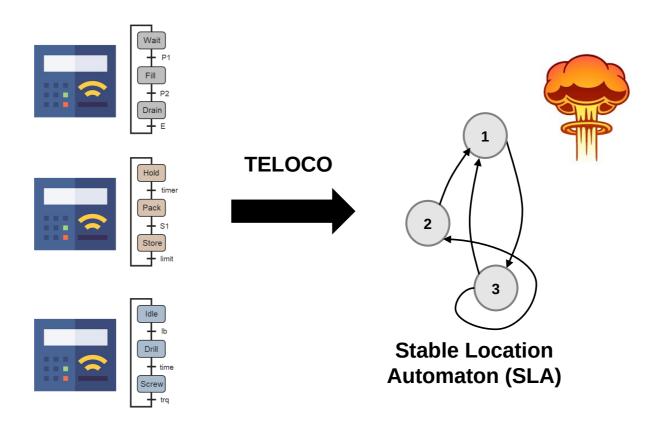


 $\texttt{Tennessee-Eastman} \rightarrow \texttt{}$





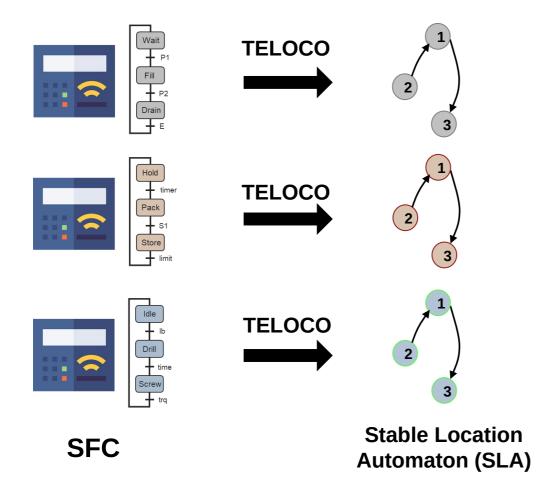




SFC





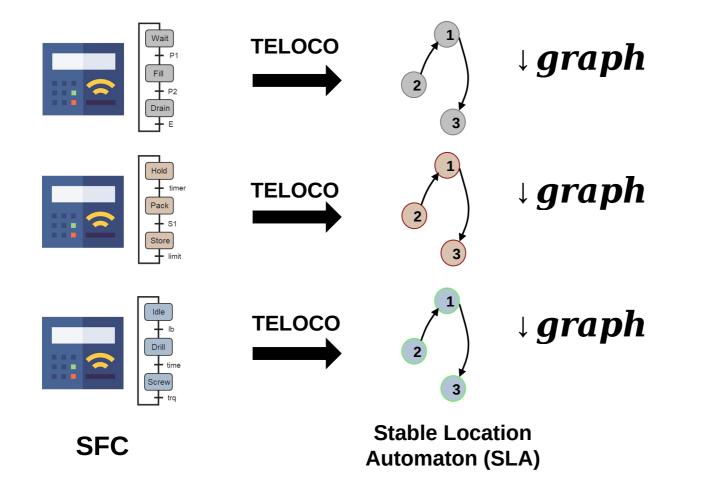


Decomposition





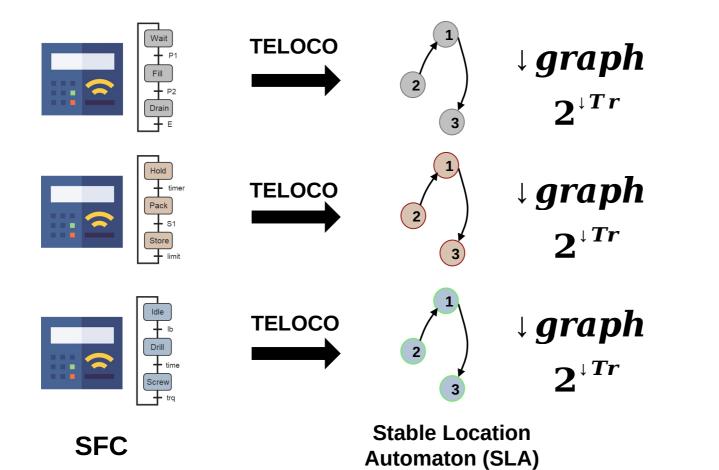






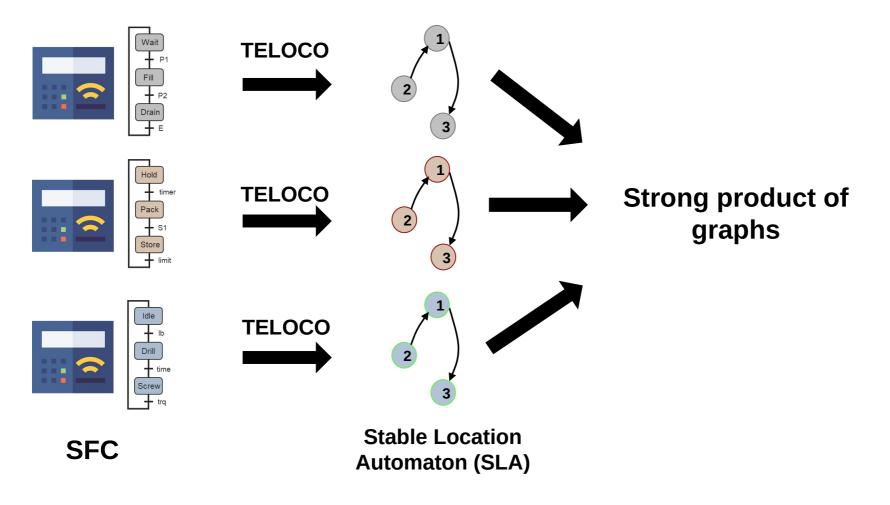






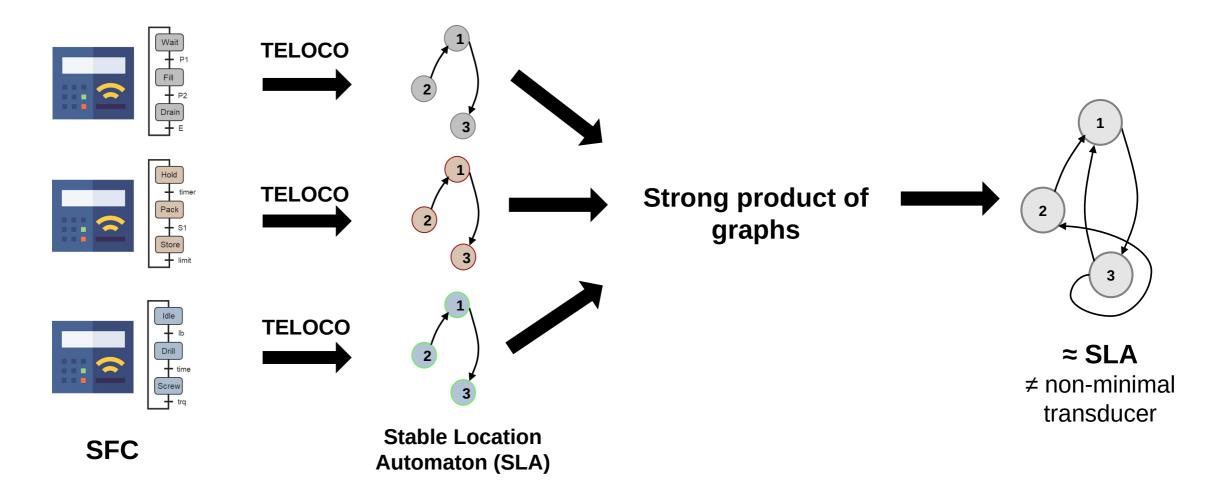


















	Strong Product	SLA
4 graphs	2 636 ms	1 091 838 ms
5 graphs	43 420 ms	X
6 graphs	2 223 811 ms	Х
8 graphs	X	X

Memory limitation (375Gb RAM)







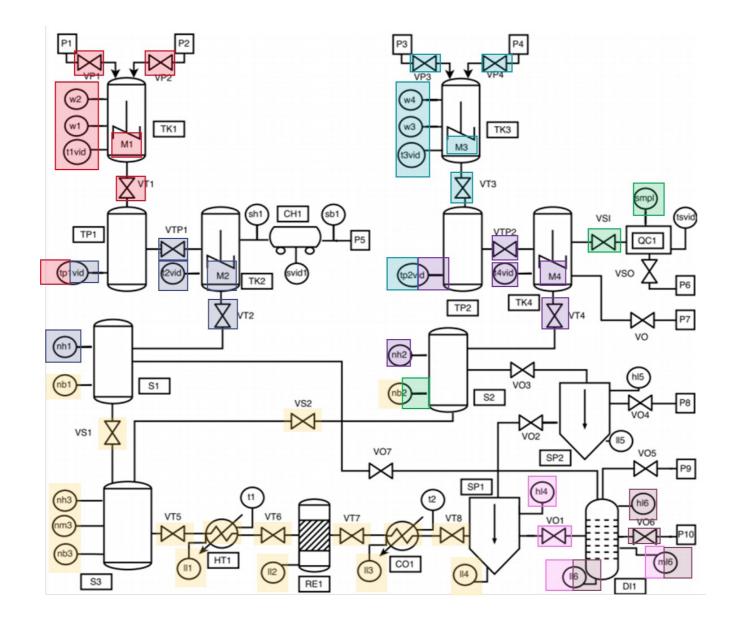
	Strong Product	SLA
4 graphs	2 636 ms	1 091 838 ms
5 graphs	43 420 ms	X
6 graphs	2 223 811 ms	Х
8 graphs	X	X

→ Decomposition into sub-processes





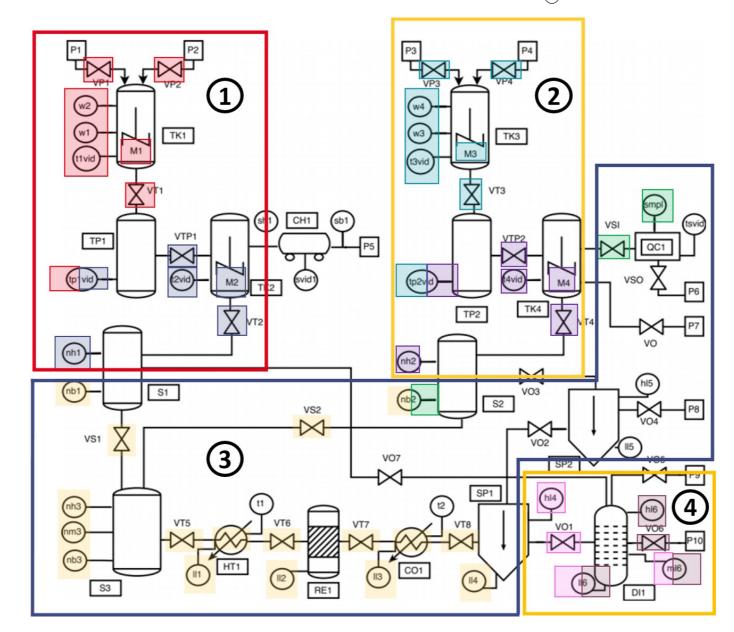






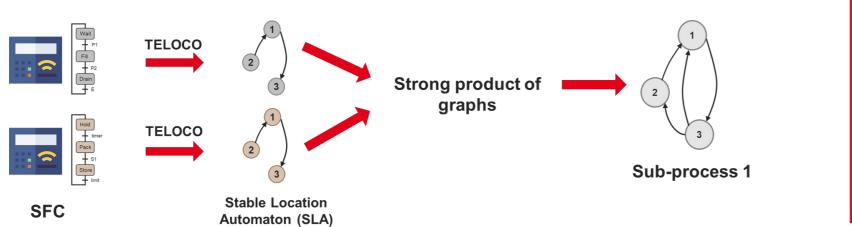


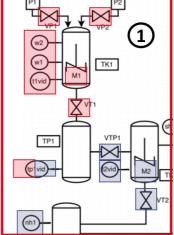




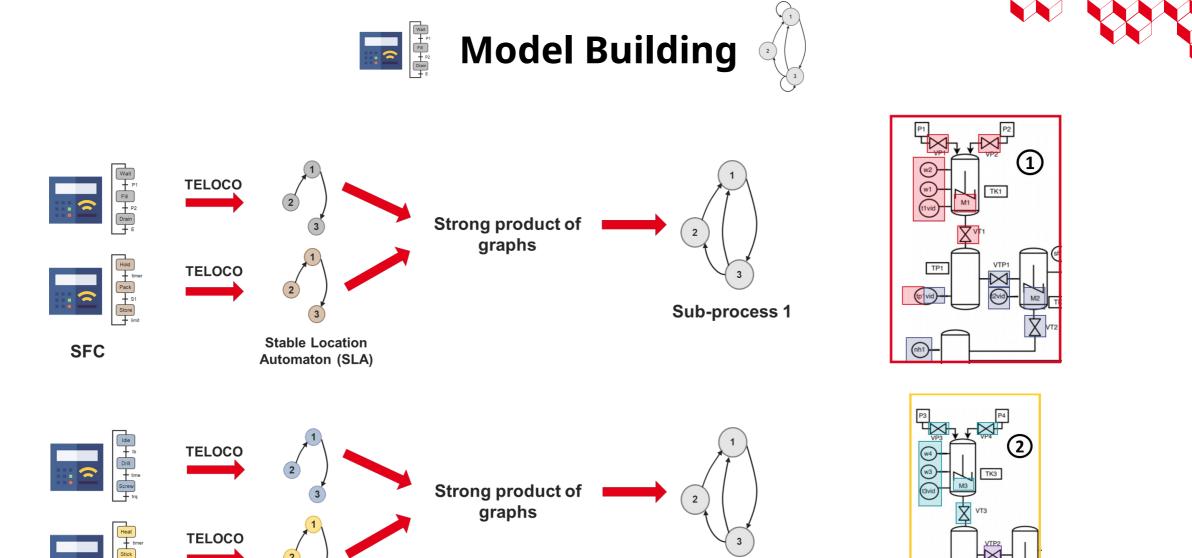












Sub-process 2



~

3

Stable Location

Automaton (SLA)

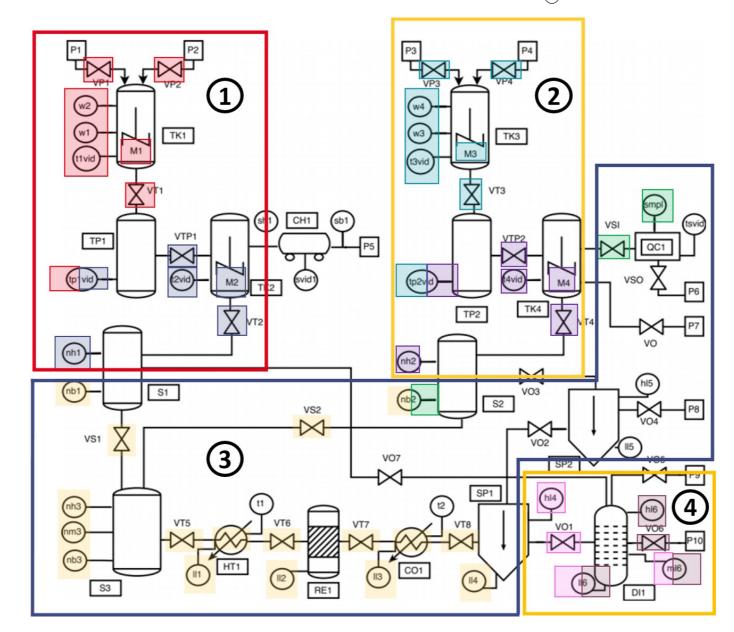
TK4

TP2

nh2



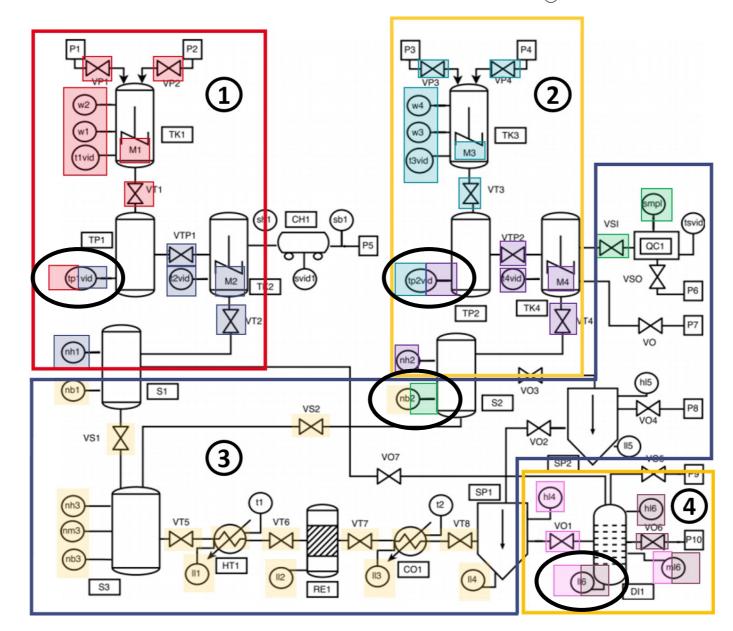




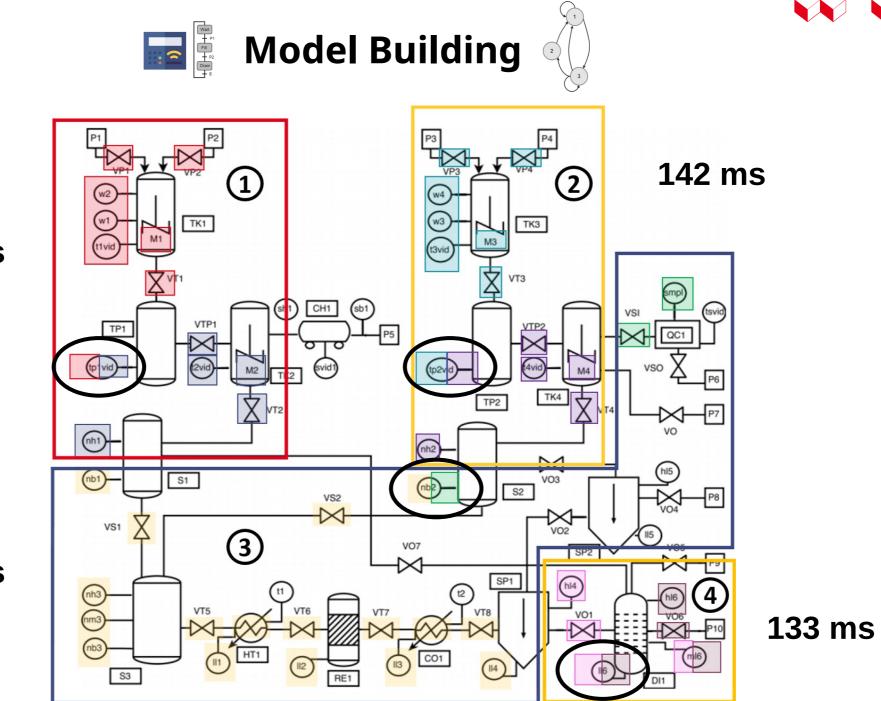








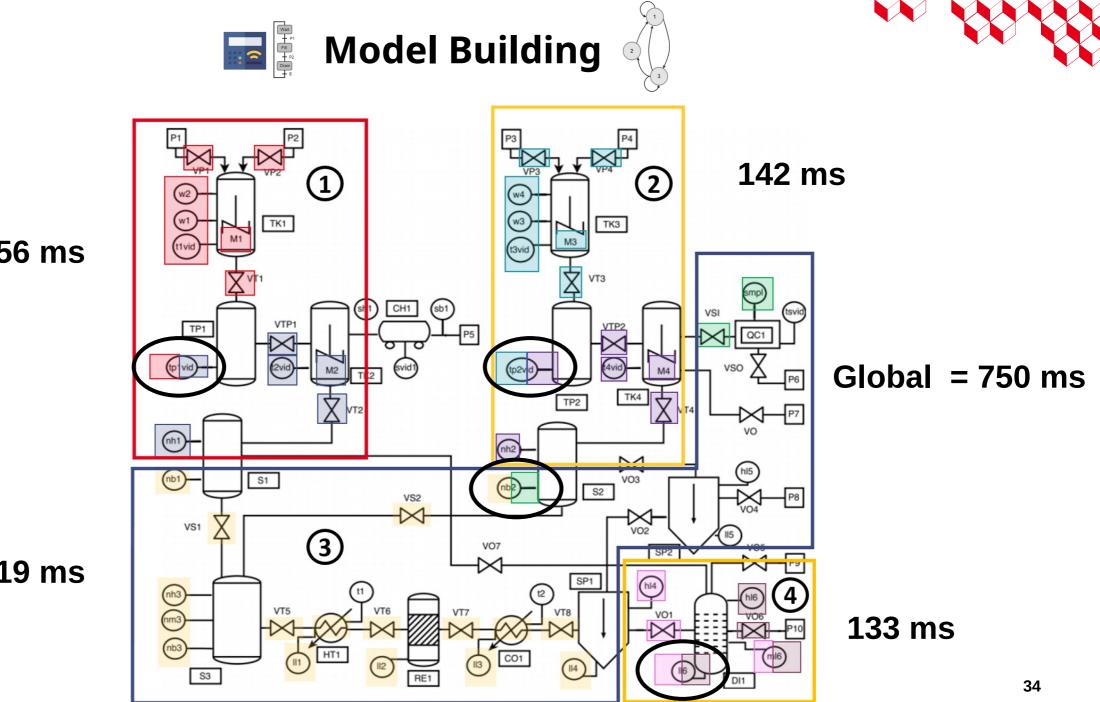




156 ms

319 ms





156 ms

319 ms

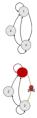


Contents



Identifying Cybersecurity Risk for System Safety

PLC-Logic Based Cybersecurity Risk Identification



- Model building
- Threat model application

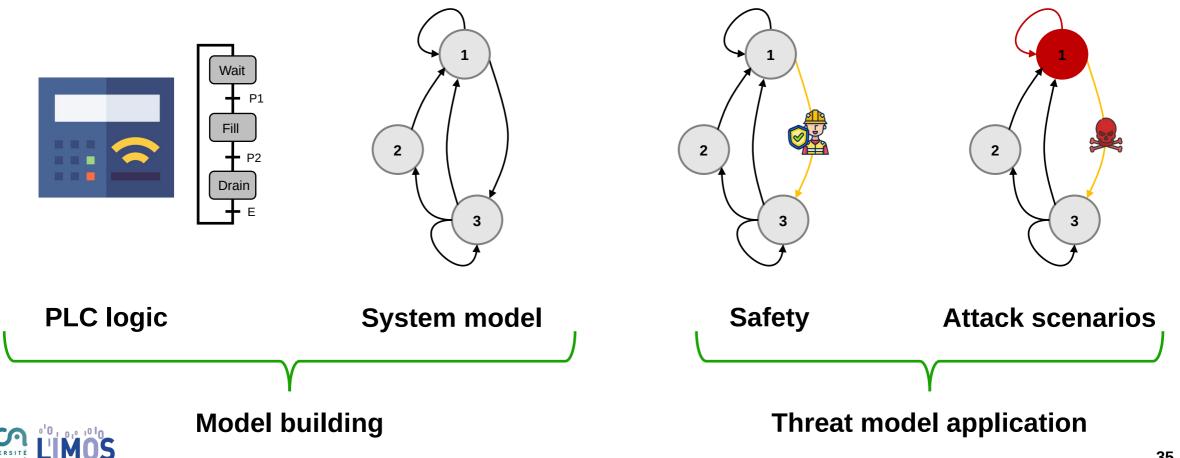




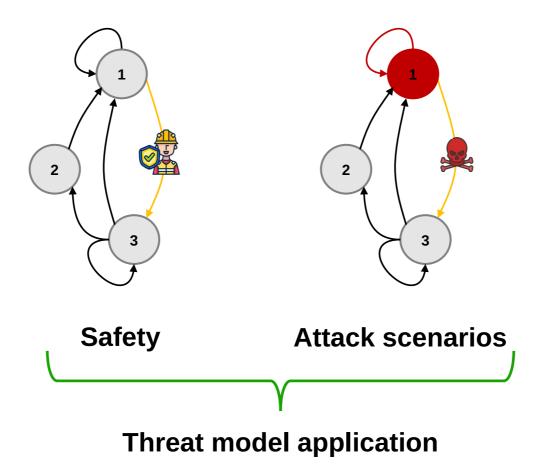


Auveran

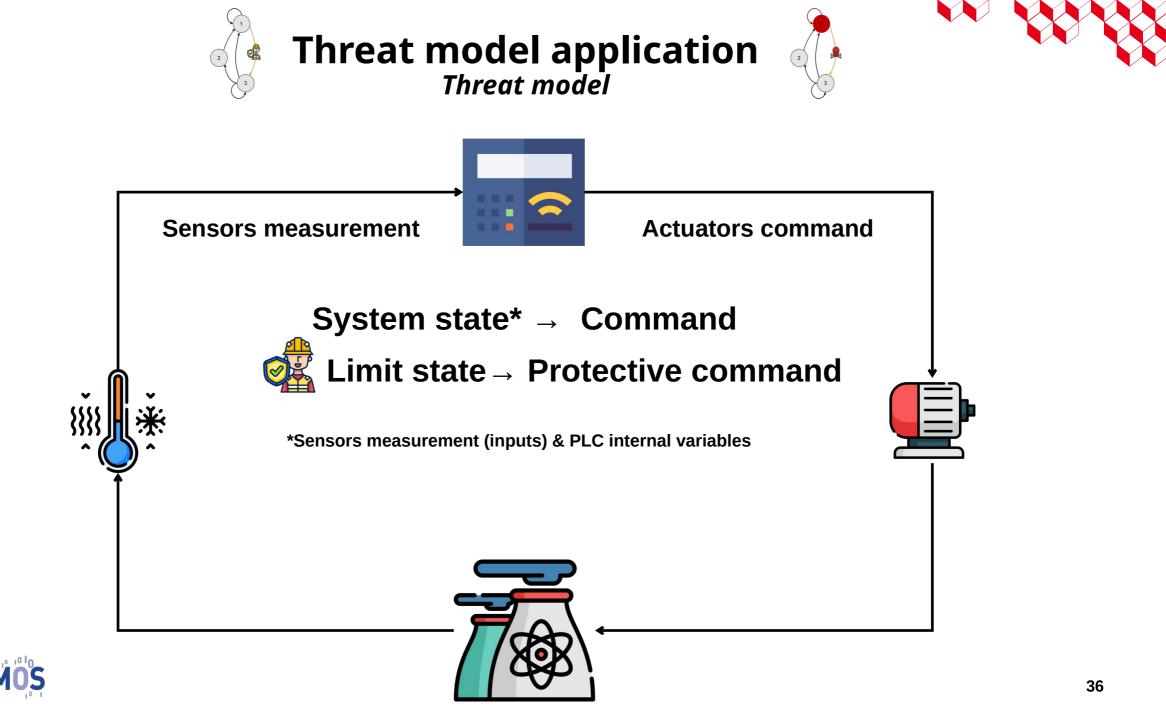
PLC-Logic Based Cybersecurity Risk Identification













Threat model application







Sensor A & Actuator 1



Process Hazard Analysis (PHA)



(Sensors B & /C) & **/Actuator 2**



Sensors B & /C Actuator 2

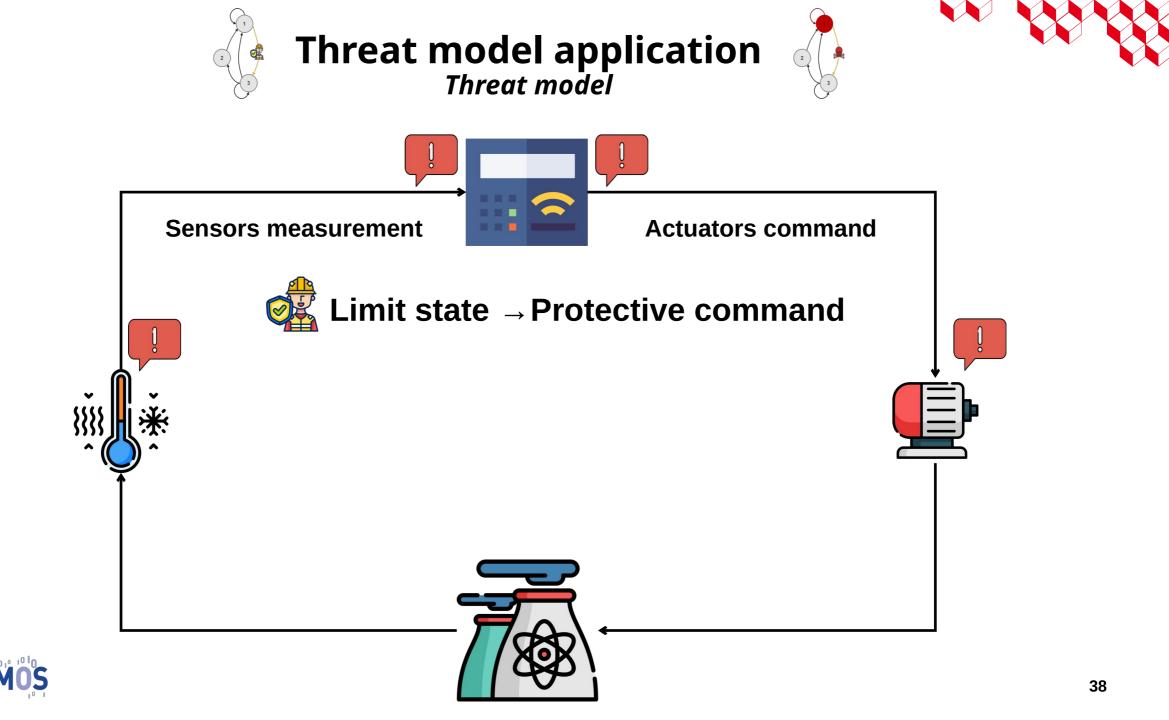


Sensor D & (Actuators 3 | 4)

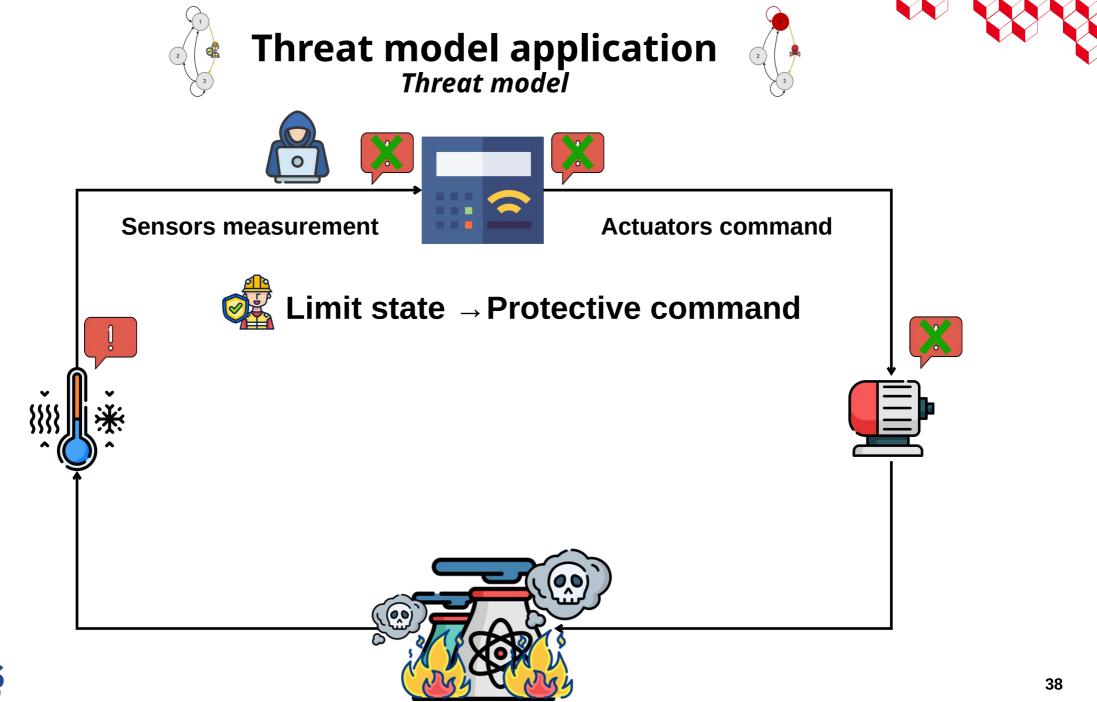


Sensor D /Actuator 3 & /Actuator 4

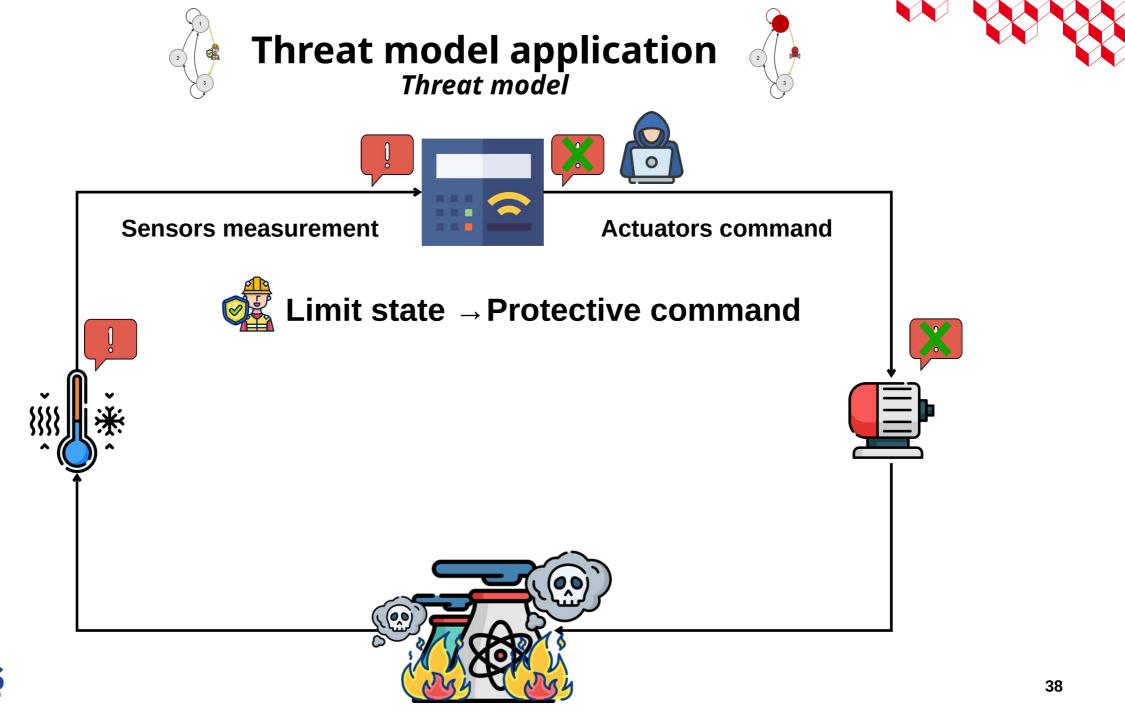




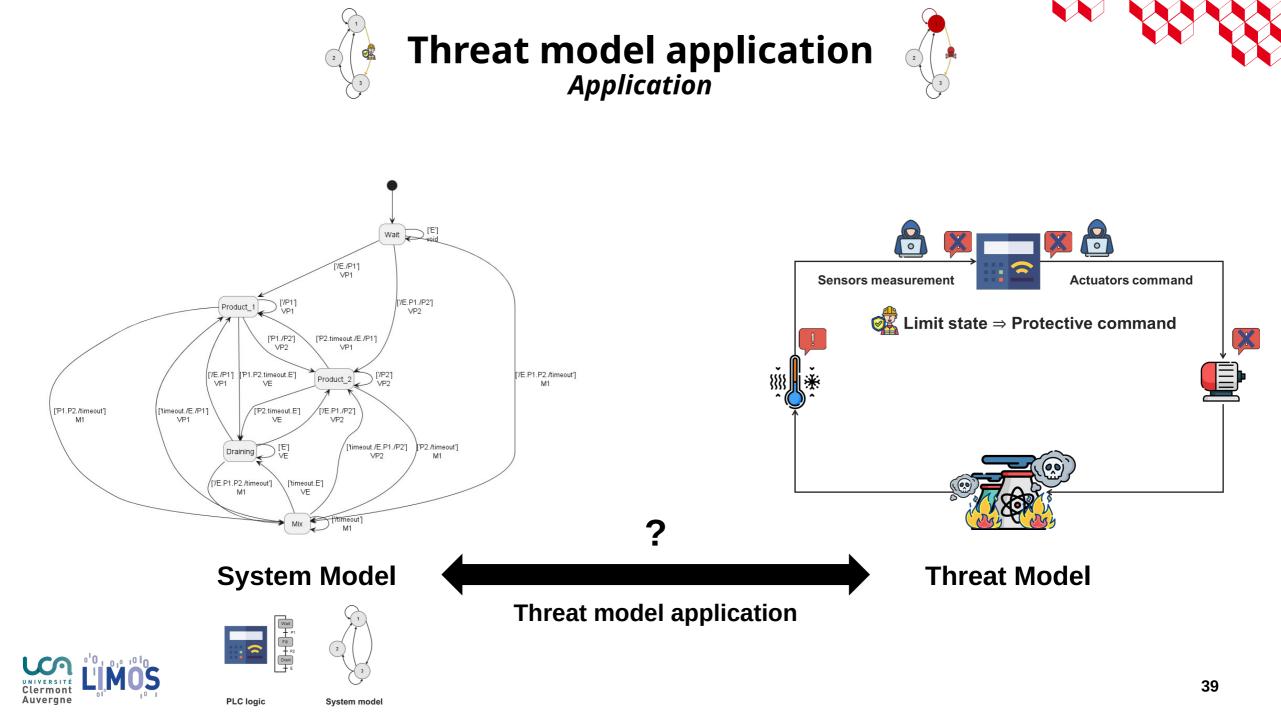
Auverane

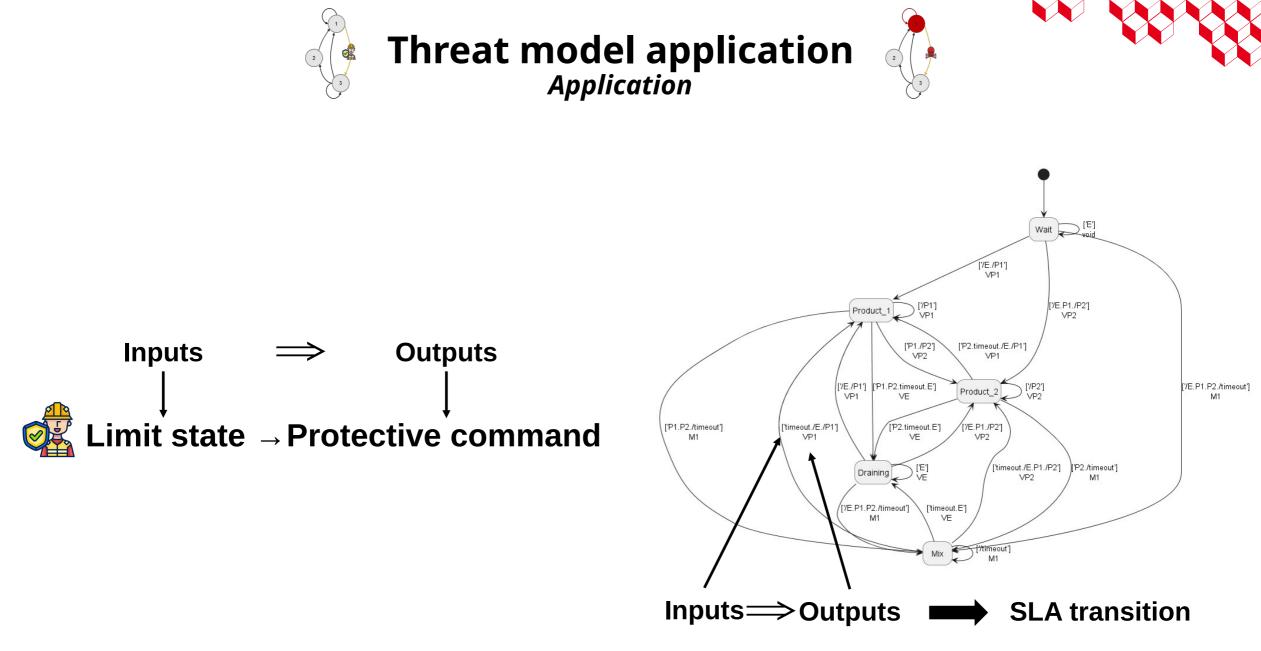








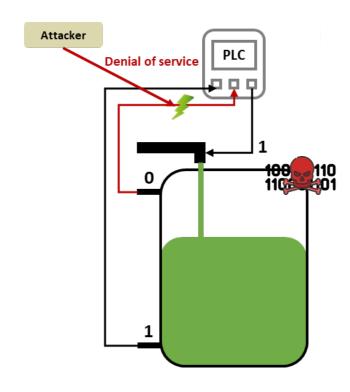








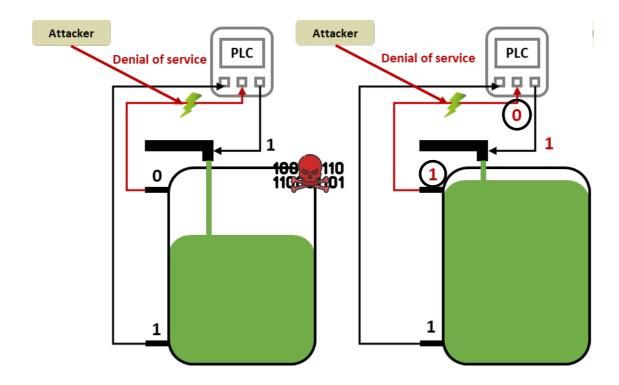








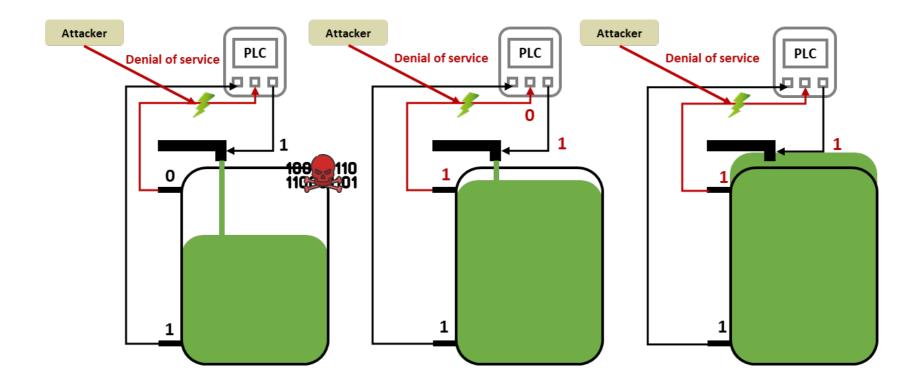






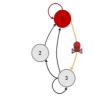


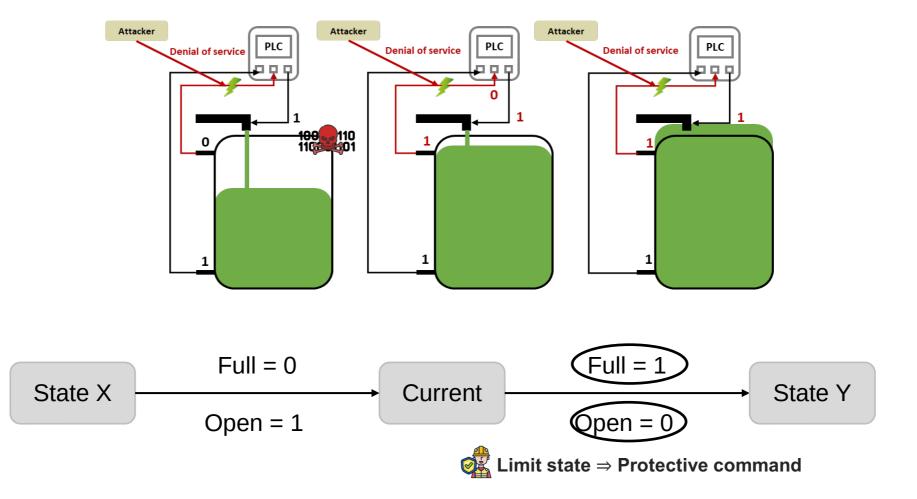








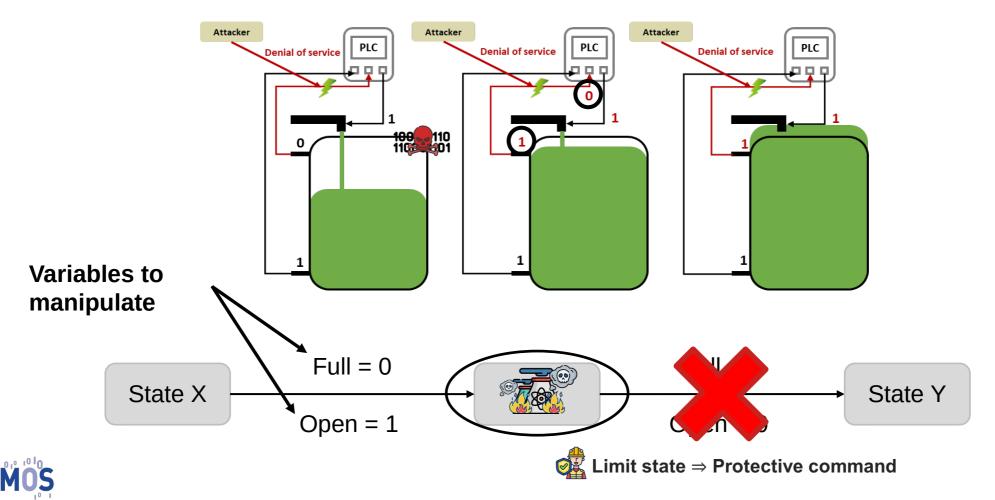








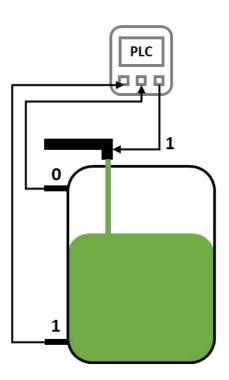
Block a state change



Auvergne

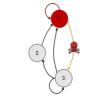


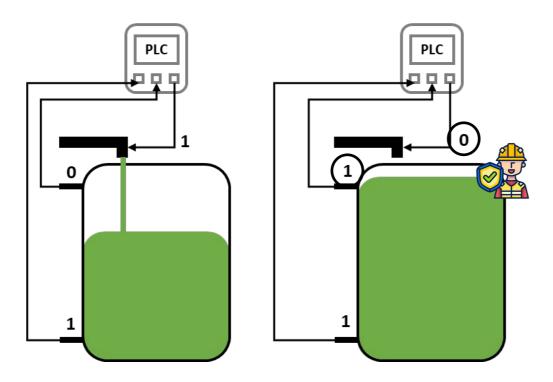








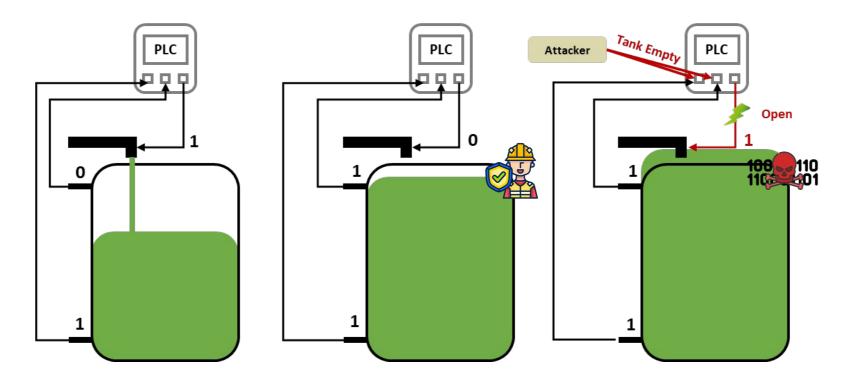






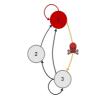


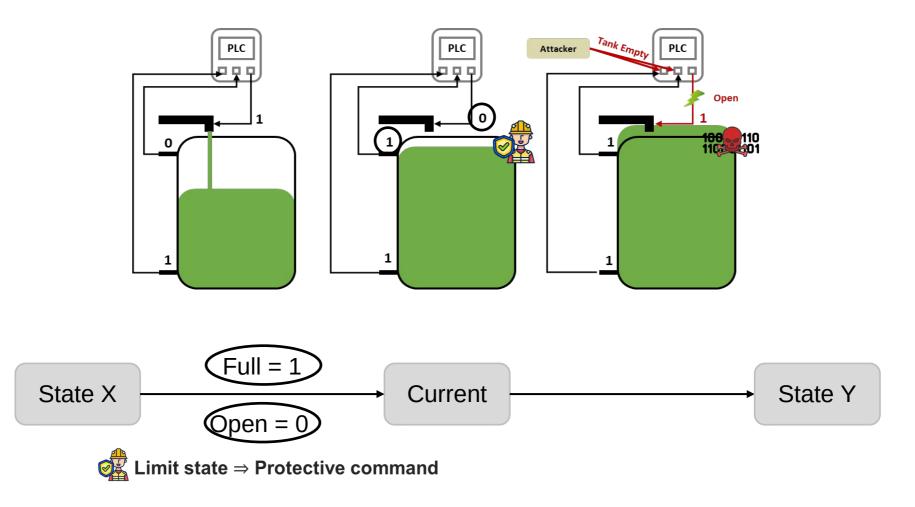






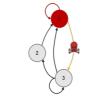


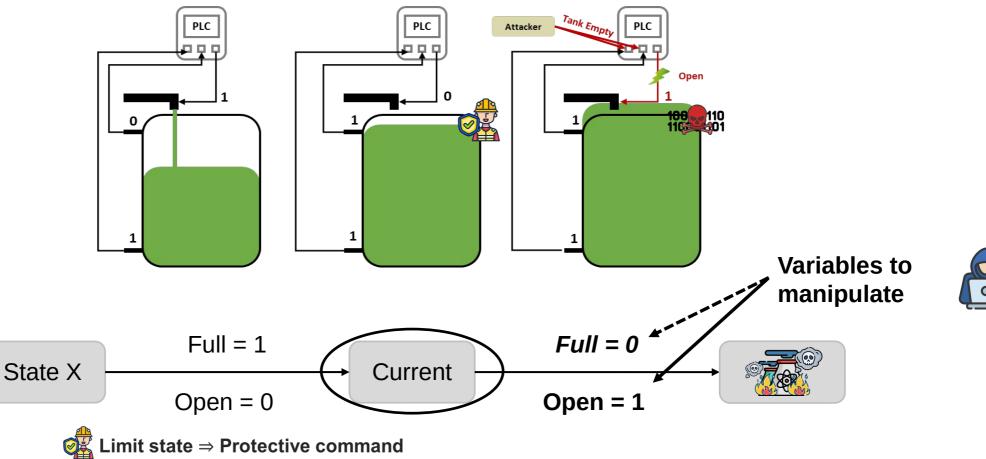






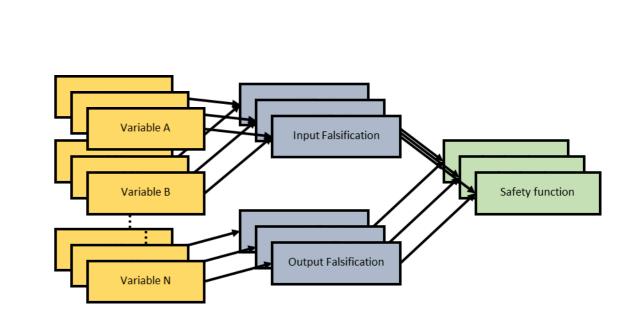








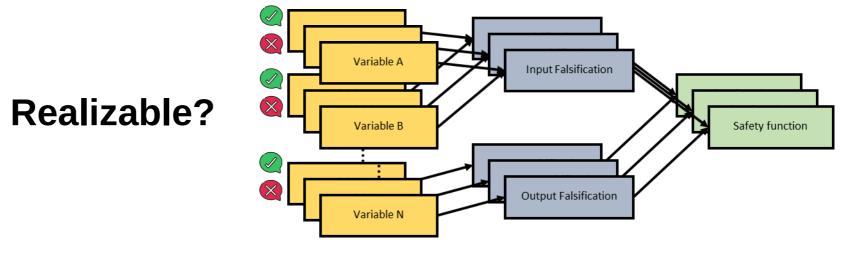




Theoretical Attack Scenarios



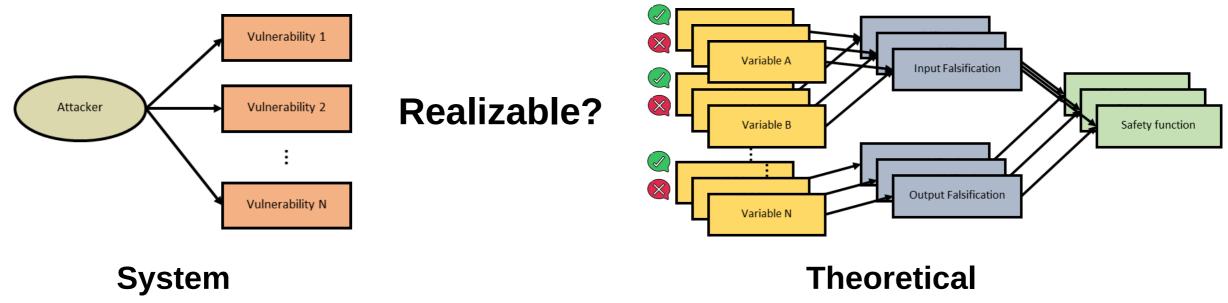




Theoretical Attack Scenarios



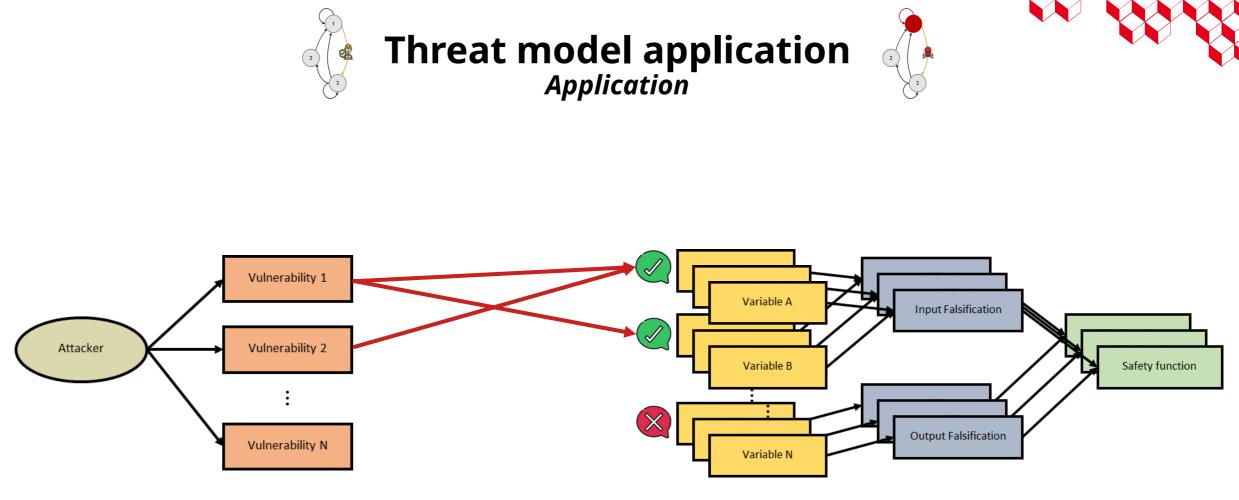




Vulnerabilities

Attack Scenarios





System Vulnerabilities

Theoretical Attack Scenarios



Contents



Cybersecurity Risk Assessment for System Safety



What an attacker can do



What an attacker might do



Is it serious ?



Identifying Cybersecurity Risk for System Safety



Literature Review & Classification



PLC-Logic Based Cybersecurity Risk Identification



Conclusion and perspectives



Conclusion & Perspectives



- → Main Goal: Predict impacts of cyberattacks on safety
 - \rightarrow "Is this cyberattack impacting the real world?"
- \rightarrow Attempts to model large industrial control systems
 - \rightarrow Still facing combinatorial explosion
 - \rightarrow But able to represent realistic-ish systems
- \rightarrow A very simplified attacker model based on safety protective commands

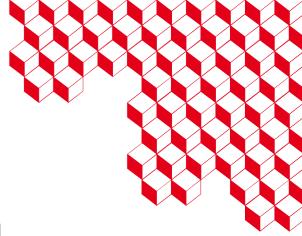
Perspectives:

 \rightarrow Take into account other PLC program languages (Ladder, FBD, etc) and discrete/continuous variables:

- \rightarrow Will most likely involve SMT solvers and optimization techniques
- → Consider more powerful attacker models:
 - \rightarrow Not limited to 1 step...
 - $\rightarrow\,$ Attack trees, Markov chains, Dolev Yao intruder, etc







Thank you for your attention



Picture by tasukaran from Pixabay - Pictograms designed by Freepik - Domino effect icons created by lutfix – Flaticon -State of the art icons created by Three musketeers - Flaticon



Conclusion & Perspectives



International Peer-Reviewed Conferences with Proceedings

<u>M. Da Silva</u>, M. Puys, P.-H. Thevenon, et S. Mocanu, « **PLC Logic-Based Cybersecurity Risks Identification for ICS** », in *Proceedings of the 18th International Conference on Availability, Reliability and Security*, Benevento Italy: ACM, août 2023, p. 1-10. doi: <u>10.1145/3600160.3605067</u>.

<u>M. Da Silva</u>, M. Puys, P.-H. Thevenon, S. Mocanu, et N. Nkawa, « **Automated ICS template for STRIDE Microsoft Threat Modeling Tool** », in *Proceedings of the 18th International Conference on Availability, Reliability and Security*, Benevento Italy: ACM, août 2023, p. 1-7. doi: 10.1145/3600160.3605068.

International Peer-Reviewed Journals (under review)

M. Da Silva, M. Puys, P.-H. Thevenon, et S. Mocanu, Safety-Security Convergence: Automation of IEC 62443-3-2, Computers & Security.

National Events (RESSI)

M. Da Silva, M. Puys, P.-H. Thevenon, et S. Mocanu, Automatisation de l'analyse des risques de cybersécurité des systèmes industriels. In Rendez-Vous de la Recherche et de l'Enseignement de la Sécurité des Systèmes d'Information, RESSI 2022, Chambon-sur-Lac, France, 2022.

<u>M. Da Silva</u>, M. Puys, P.-H. Thevenon, et S. Mocanu, **Convergence sûreté-sécurité des Systèmes de Contrôle Industriel**. In *Rendez-Vous de la Recherche et de l'Enseignement de la Sécurité des Systèmes d'Information, RESSI 2024, Eppe-Sauvage, France*, 2024.

Patent

Mike Da Silva, Pierre-Henri Thevenon, Maxime Puys, Stéphane Mocanu. **Procédé et dispositif d'identification des risques de cyberattaques**. France, N° de brevet: FR3144828. 2024. **Method and device for identifying risks of cyberattacks**. United States, Patent n° : US20240211607A1. 2024.